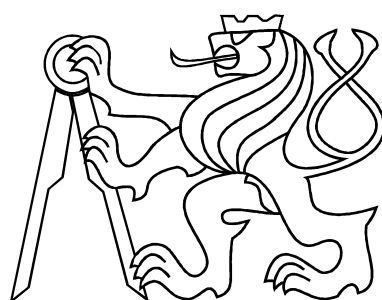


CZECH TECHNICAL UNIVERSITY IN
PRAGUE

Faculty of Nuclear Sciences and Physical
Engineering

Department of Physics



Research Project

**Detector Control System for the ALICE
Experiment**

Miroslav Šimko

Supervisor: Doc. RNDr. Vojtěch Petráček CSc.

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Title:

Detector Control System for the ALICE Experiment

Author: Miroslav Šimko

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Supervisor: Doc. RNDr. Vojtěch Petráček CSc.

Consultant: Ing. Čeněk Zach

Abstract:

This paper describes the Detector Control System (DCS) for the Silicon Drift Detector (SDD), especially the software part of the system.

A part of this document is a description of the distribution of the system between the four SDD DCS computers. Moreover, the FSM tree is illustrated with all its changes.

What is more, all the changes to the system that were made between September 2011 and August 2012 are described as well. The main upgrades were migrating of the SDD DCS servers, the new FSM state `BEAM_TUNING`, improvements in the supervising of the voltage supply, and new humidity sensors.

Key words:

control system, DCS, ALICE, ITS, SDD, PVSS

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Chapter 1

Introduction

1.1 Overview

This paper describes in general the Detector Control System (DCS) of the Silicon Drift Detector (SDD) which is a part of the Inner Tracking System (ITS) of the ALICE experiment at the LHC. Moreover, it summarizes the changes to the SDD DCS that were made between September 2011 and August 2012.

1.2 ALICE experiment

ALICE (A Large Ion Collider Experiment) [1, 23] is a general-purpose heavy-ion detector at the CERN Large Hadron Collider. It is designed to study quantum chromodynamics (QCD), the strong interaction sector of the standard model. The main goal of ALICE is to study physical properties of the quark gluon plasma (QGP), possibly a state of matter that existed a few microseconds after the beginning of the universe. The detector is composed of 18 sub-detectors and their associated supply systems. In Fig. 1.1 the layout of ALICE is shown.

The central part of the detector is barrel shaped and is situated in a solenoid magnet which is reused from the L3 experiment at LEP. The L3 magnet provides magnetic field of 0.5 T.

From inside out, the barrel consists of Inner Tracking System (ITS), of six planes of high-resolution silicon pixel (SPD), drift (SDD), and strip (SSD) silicon detectors, a cylindrical Time-Projection Chamber (TPC), three particle identification arrays of Time-of-Flight (TOF), Ring Imaging Cherenkov (HMPID) and Transition Radiation (TRD) detectors, and two electromagnetic calorimeters (PHOS and EMCal). All the sub-detectors except HMPID, PHOS, and EMCal cover the full azimuth.

The forward muon arm consists of several absorbers, a dipole magnet, and fourteen planes of triggering and tracking chambers. What is more, there are several smaller detectors situated in smaller angles (ZDC, PMD, FMD, T0, V0). An array of scintillators (ACORDE) is used for triggering of the cosmic rays.

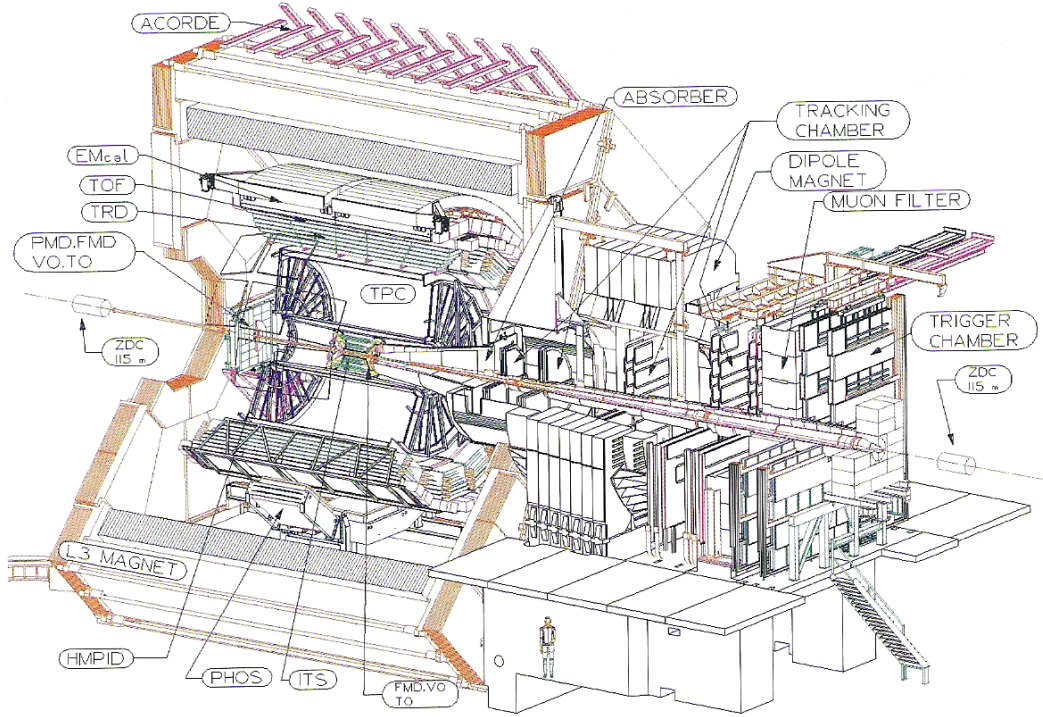


Figure 1.1: Overview of the ALICE detector [1].

1.3 Inner Tracking System (ITS)

This is the innermost group of detectors. The Inner Tracking System (ITS) [2] is composed of six layers of high resolution silicon detectors (see Fig. 1.2) – two layers of silicon pixel detectors (SPD), two layers of silicon drift detectors (SDD), and two layers of silicon strip detectors (SSD).

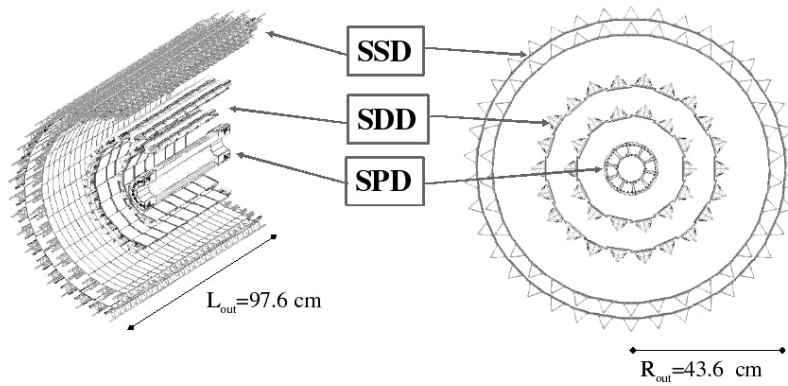


Figure 1.2: Layout of the Inner Tracking System [1].

Its main purposes are to determine the primary vertex with a resolution less than $100\ \mu\text{m}$, to reconstruct the secondary vertexes from the decays of hyperons and D and B mesons, to track and identify particles with momentum below $200\ \text{MeV}/c$, to improve the momentum and angle resolution for the Time-Projection Chamber (TPC) and to reconstruct particles that cross the dead regions of TPC.

1.4 Silicon Drift Detector (SDD)

The Silicon Drift Detectors (SDD) [2, 21] make the two intermediate layers of the ITS (see Fig. 1.2) in which the particle density is expected to reach $7\ \text{cm}^{-2}$. They were chosen for their very good multi-track capability and because they provide, along with the silicon strip layers, two out of four dE/dx samples needed for the ITS particle identification.

In the drift detectors, the detection is made by measuring the transport time of charge, released during traversing of a particle at a certain spot, and reconstructing (in one dimension) this spot. The SDDs provide very high resolution at the cost of the readout speed (a few μs).

Table 1.1: Main parameters of the ALICE SDD layers and ladders [1].

	layer 3	layer 4
Detectors per ladder	6	8
Ladders per layer	14	22
Detectors per layer	84	176
Ladder sensitive half-length (cm)	22.16	29.64
Average ladder radius (cm)	15.03	23.91
Ladder space-frame weight (g)	11	15
Weight of ladder components (g)	87	121

The two SDD layers are divided into 260 modules, each consisting of one silicon drift detector and two front end hybrids, connected to an end-ladder LV board. The modules are mounted on linear structures called ladders. There are 14 ladders with six modules each on layer 3, and 22 ladders with eight modules each on layer 4. The ladder space frame is made of carbon-fiber reinforced plastic and has a protective coating against humidity.

1.5 Detector Control System (DCS)

The main objective of the ALICE Detector Control System (DCS) [3, 4] is to ensure safe and correct operation of the ALICE experiment. It provides remote control in such a way that the whole ALICE experiment can be operated from a single workplace (ALICE Control Room – ACR at LHC point 2). The DCS was designed to reduce the downtime of the experiment, and therefore, contribute to high running efficiency. Although being developed by various groups in parallel, the DCS is a coherent and homogeneous system.

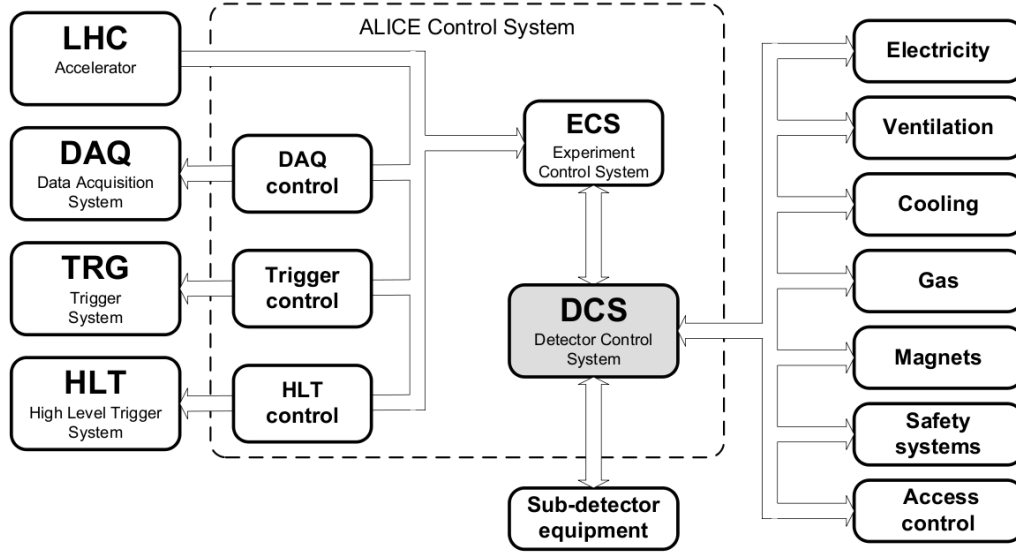


Figure 1.3: The ALICE online systems [3].

The DCS is a part of the ALICE Control System. As shown in figure 1.3, the ALICE Control System includes all control activities in the ALICE experiment: the Experiment Control System (ECS), the DCS, the Data Acquisition (DAQ), the Trigger System (TRG) and the High-Level Trigger (HLT – see [3] or [23]). The DCS takes care of interfering with the various services of the sub-detectors (such as cooling, electricity, magnets, safety, etc.). The ECS is responsible for the synchronization of the various systems, i.e. DCS, DAQ, TRG and HLT.

1.5.1 Hardware architecture

The hardware architecture is divided into three layers (see figure 1.4). The ‘supervisory layer’ is composed of PCs that provide user interfaces to the operators and are connected to the disk servers (that hold databases, archiving, etc.). The DCS also interferes with external systems through this layer via the DIP protocol (Data Interchange Protocol) which is a protocol defined in CERN that allows exchanging of information between various systems.

The supervisory layer interfaces to the ‘control layer’ mainly through a LAN. This layer also consists mainly of PCs that interface to the experimental equipment, but also of the PLCs or PLC-like structures. These devices collect information from the lower, so called ‘field’, layer and make the detector equipment available for the supervisory layer. The control layer interfaces to the equipment in the field layer through fieldbuses, but also via the LAN.

The field layer contains all field devices (such as power supplies, fieldbus nodes, etc.), sensors and actuators, etc. It is designed to avoid sharing of devices between different sub-detectors so they can run simultaneously and concurrently.

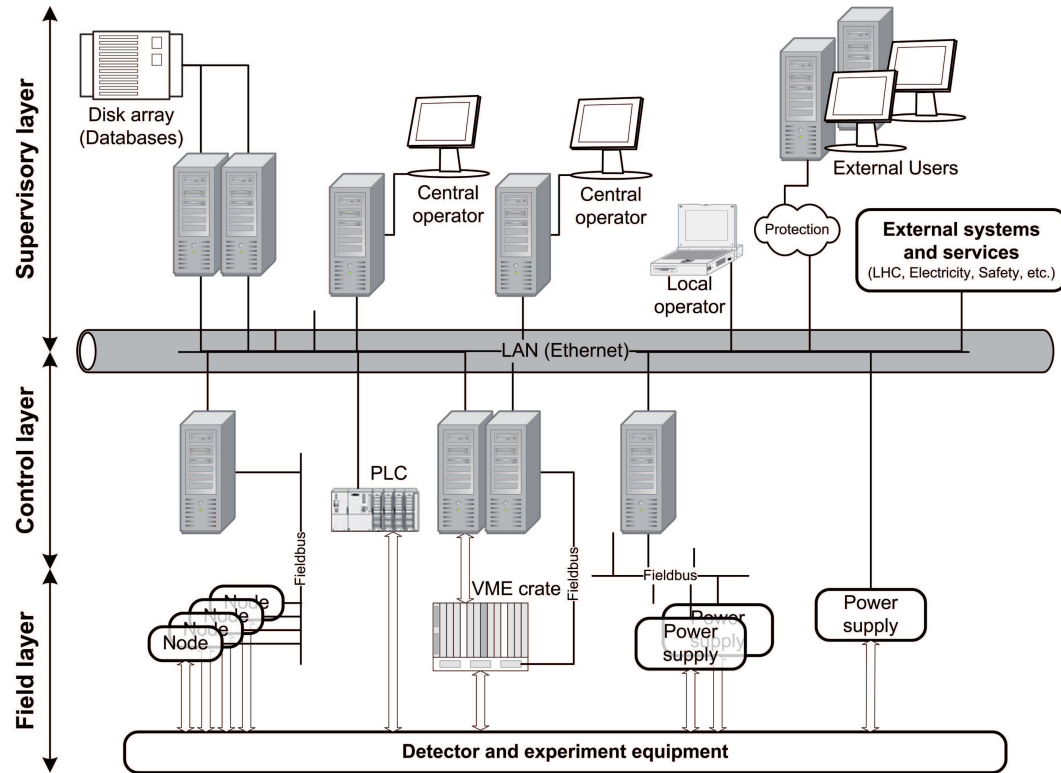


Figure 1.4: DCS hardware architecture [3].

1.5.2 Software architecture

The core software of the DCS is a commercial SCADA¹ (Supervisory Controls and Data Acquisition) program PVSSII [10].

The control system is built using the 'JCOP framework' which contains Finite State Machine functionality (see below), drivers for different types of hardware, communication protocols, and configurable components for frequently used applications such as low voltage power supply, etc. The framework also includes many other utilities such as interfaces to the various databases (configuration, archiving), visualization tools, access control, alarm configuration and reporting, etc. The JCOP framework is being developed by a joint effort between all the LHC experiments.

Several add-ons to this framework exist specially for the ALICE specific needs. The various layers are shown in figure 1.5.

PVSSII, the framework and the user applications are designed to work mainly on Microsoft Windows and Linux platforms. Some limitations, however, may exist for some Windows specific features, when using Linux.

¹As the name indicates, SCADA (Supervisory Controls and Data Acquisition) are programs, designed to control and collect data from various hardware devices. They are not meant to be the full control systems, but focus on the supervisory level. As such, they are purely software products positioned on top of the hardware to which they are interfaced via PCs or PLCs [13].

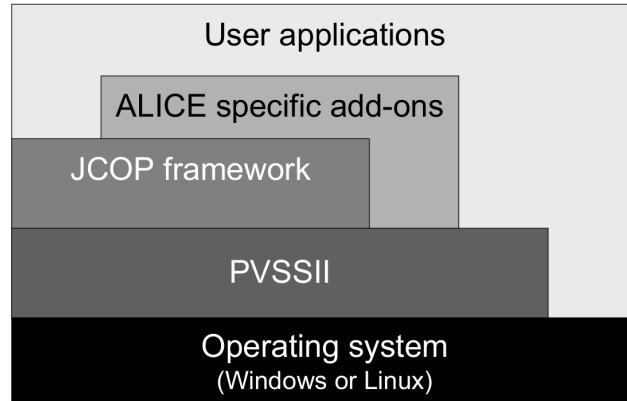


Figure 1.5: Overview of the software layers in the control system [3].

Finite State Machine (FSM)

The hierarchical control structure is a tree-like structure composed of, so called, units. The units' behavior is modeled by the Finite State Machine (FSM) [12]. It is an intuitive, generic mechanism to program behavior of a piece of equipment or a sub-system.

There are three types of units: Device Units (DU), Control Units (CU), and Logical Units (LU). The Device Units are units with no children. They take care of a piece of hardware directly. The Logical Units integrate several Device units in a group. Finally, the Control Units are units that have children which may be DUs, LUs, and even CUs.

Every object in the FSM has a set of 'states' between which it can switch by performing 'actions'. The states propagate 'up' the FSM tree which means that the parent units react to the change of states of the children units. The actions propagate 'down' the tree so that when the parent unit performs an action the children units react to it (see Fig. 1.6).

Datapoint concept

The PVSS [6, 11] has its own run-time database, which allows storing data from the hardware devices. This database is designed in such a way that the data are easily accessible and can be treated as variables. Therefore, it has to be optimized for fast access. However, the stored data are difficult for accessing from outside the PVSSII. That is why the JCOP framework also includes an archiving tool.

The device data in the PVSS run-time database are structured as, so called, 'DataPoints' (DP) of their predefined 'DataPoint Types' (DPT). The DPs/DPTs allow to model the devices by defining the DPs' structure. As such, the data associated with a particular device can be grouped together, instead of being held as separate variables. To interfere with the data in the DPs, PVSSII has a special editor called 'PARA'. It is also possible to interfere with them via scripts.

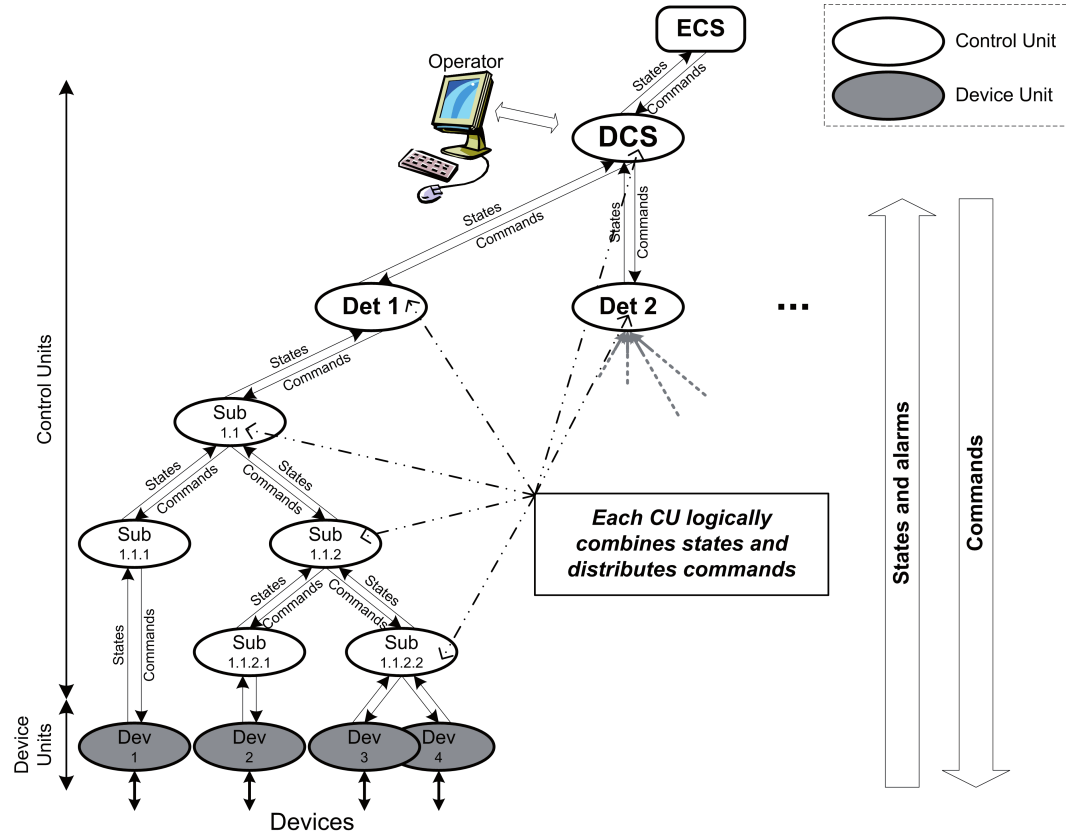


Figure 1.6: DCS hierarchical control architecture [3].

OPC and DIM servers

The OPC (Object Linking and Embedding for Process Control) [6, 14] is a means of controlling a piece of hardware. It provides another abstraction level between hardware and a SCADA system (e.g. PVSS). Therefore, the OPC client works in a similar way as e.g. the drivers on a printer. This is extremely helpful because the developer of a control system does not have to read the registries of HW, etc.

Many vendors of equipment commonly used in the physics experiments provide OPC servers together with their HW. This is the case of CAEN, WIENER and ISEG which is the manufacturer of the SDD high voltage supply.

The OPC servers, although very useful, are quite uneasy to develop. That is why CERN has produced the DIM (Distributed Information Management) protocol [15] which provides a similar abstraction level to the OPC. The PVSS is equipped with a DIM toolkit that helps the developers to connect the equipment to the PVSS datapoints.

Chapter 2

Detector Control System for the SDD

In this chapter we describe the Detector Control System for the Silicon Drift Detector. Because the hardware part is already documented in [5] and [23], in this paper we focus on the software part of the system.

2.1 SDD DCS computers

The SDD employs four computers as its DCS servers. Three of them (with the host names `alidcscom817`, `alidcscom818` and `alidcscom820`) have been recently migrated, and one stays on the old server (`alidcscom152`). For more information on migrating the servers see Section 3.1. All these servers are accessible from the computer `alidcscom001` that is placed in the CERN network. The properties of the DCS computers are summarized in Tab. 2.1.

Table 2.1: Properties of the SDD DCS computers.

Host name	Operating system	PVSS system
<code>alidcscom817</code>	Windows XP	<code>sdd_ui</code>
<code>alidcscom818</code>	Windows XP	<code>sdd_dcs</code>
<code>alidcscom152</code>	Windows XP	<code>sdd_infra</code>
<code>alidcscom820</code>	Linux	no PVSS

2.1.1 Server `alidcscom817`

The `alidcscom817` is dedicated for the user interface of the SDD DCS. This is where the detector is supervised by an operator. The PVSS system on this computer is named `sdd_ui`.

On this computer all the voltages are being set, the front-end electronics and readout (FERO) are turned on and off, the ventilation and cooling are controlled and humidity and pressure are supervised, everything through a set of UI panels

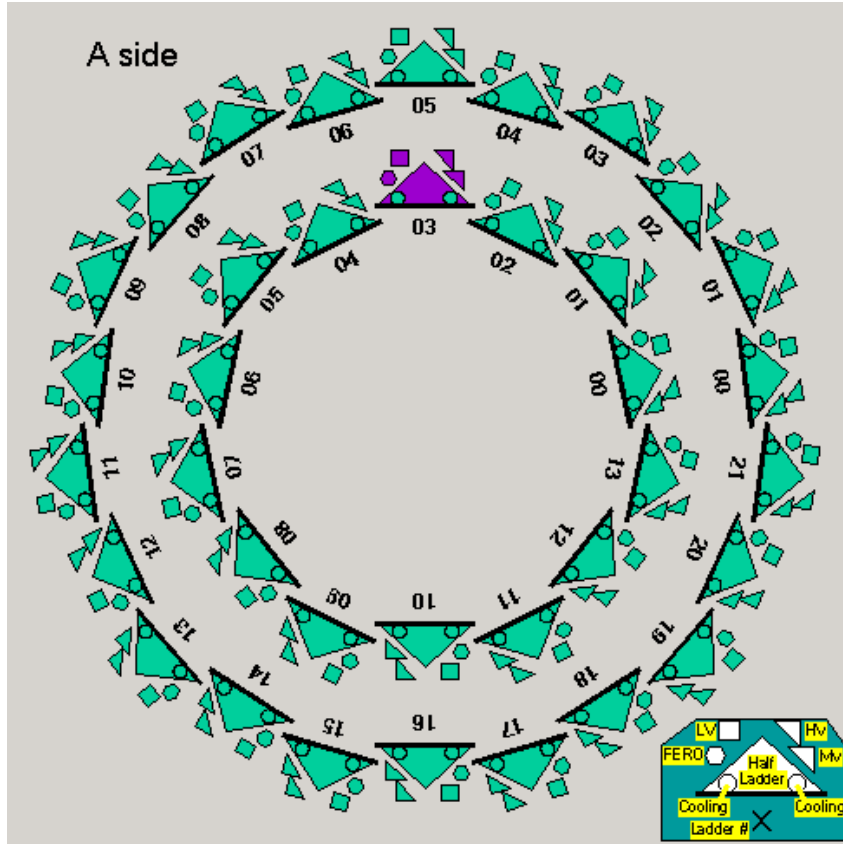


Figure 2.1: A part of the main panel of the SDD DCS user interface on `alidcscom817`, showing all the half-ladders on the A side of the detector (the anti-clockwise side according to the LHC ring).

written in PVSS (an example is in Fig. 2.1). The voltages, pressure and humidity values are drawn into trending plots, also accessible from this server.

A lot of effort is being made so that almost everything is being supervised on `alidcscom817`, however the automatic control is done by other computers.

2.1.2 Server `alidcscom818`

On this server the control of the low voltage (LV), cooling and ventilation (CaV) takes place. The PVSS system on `alidcscom818` is named `sdd_dcs`.

2.1.3 Server `alidcscom152`

On server `alidcscom152` the system `sdd_infra` (for infrastructure) is placed. This computer controls the high voltages. Moreover, the OPC server is installed here. The OPC communicates with the HV supply via a PCI bus from this computer.

`alidcscom152` is the only computer that has not been migrated. For more information see Section 3.1.

2.1.4 Server alidcscom820

This is the only computer with Linux operating system which allows it to carry the SDD's DIM server.

2.1.5 Backup discs

The ALICE DCS employs two network discs with host names `Alidcsfs001` and `Alidcsfs002`.

The backup of the DCS is made on `Alidcsfs001` in the folder `Scratch\SDD`. The backup of all DCS is created regularly and all the previous backups are still kept and are named according to the date when they were created.

`Alidcsfs002` is devoted for the DCS data, but the SDD DCS is not currently using it.

2.2 FSM tree

The FSM tree is shown in Fig. 2.2. The control units are organized logically by layers, ladders, half-ladders and detectors, and aside from these, there is infrastructure of the detector organized according to the structure of the particular piece of equipment. As you can see, the logical units under the half ladders are divided into the infrastructure systems (e.g. high voltage), and after that into the detectors or chips in the case of LV.

Two device units are placed directly under the top unit `SDD`; these units are `SddDefaultConfigurator` and `sddHvControl`. `SddDefaultConfigurator` checks if the system is downloading data and returns the appropriate state. The unit `sddHvControl` is used for control of the HV channels; it triggers the control script that corrects the voltage values (more on this topic in Section 3.2).

The SDD has a set of 12 states; Three that are set by the operator:

- `READY`,
- `BEAM_TUNING` and
- `OFF`,

and nine states dedicated for moving between states or for errors:

- `STANDBY`,
- `STBY_CONFIGURED`,
- `ERROR`,
- `DOWNLOADING`,
- `MOVING_READY`,
- `MOVING_STBY_CONF`,
- `MOVING_OFF`,

- MOVING_BEAM_TUN and
- MOVING_BEAM_TUN_DOWN.

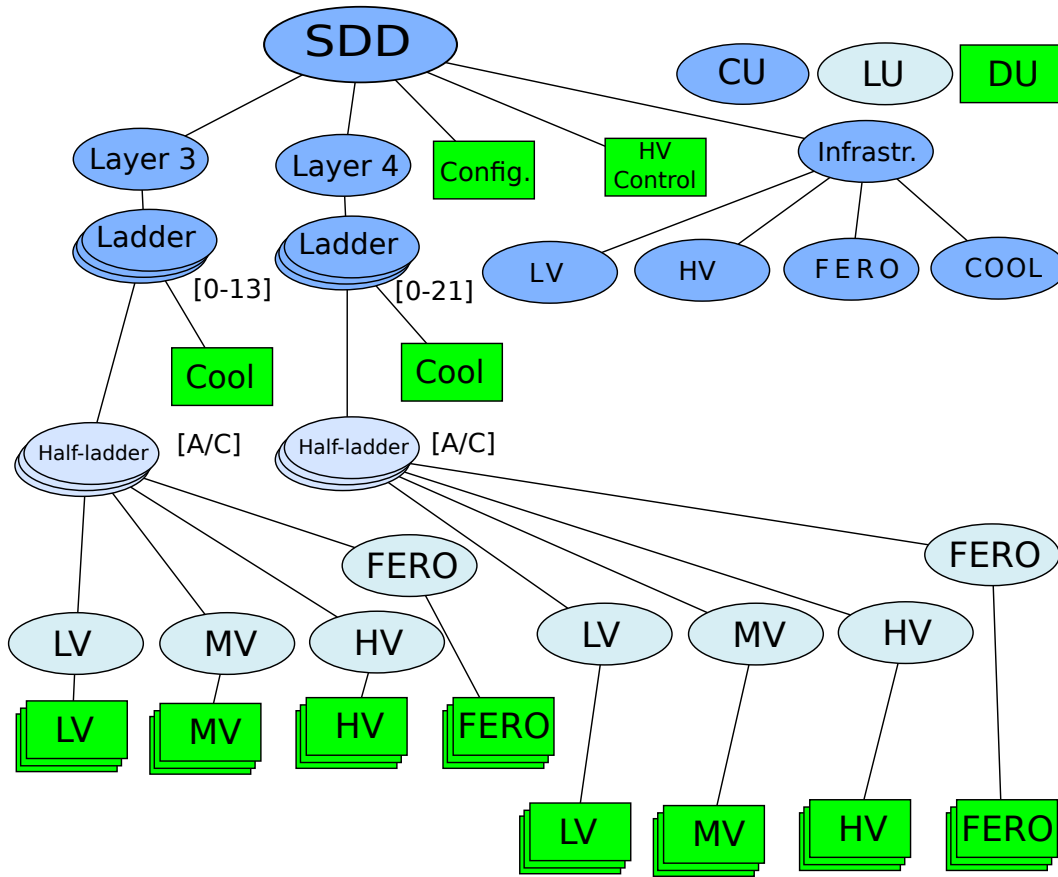


Figure 2.2: A view of the SDD FSM tree.

Chapter 3

Interventions in the SDD DCS

In this chapter we describe the changes that were made to the SDD detector control system from September 2011 to August 2012.

3.1 Migrating of the SDD DCS servers

A major upgrade has been made to the SDD DCS hardware. The system has been migrated to new, more powerful, computers. The host names of the four SDD DCS servers have been changed from ‘alidcscom150 – 153’ to ‘alidcscom817 – 820’. The new IP addresses all start with 10.160.39. and end with two digits 24 – 27. The computers ‘alidcscom817 – 819’ use Windows XP as an operating system, ‘alidcscom820’, however, uses Linux. The host names and addresses are written in Tab. 3.1.

Table 3.1: Migrating of the SDD DCS servers.

Former host name	New host name	Migrated	IP address
alidcscom150	alidcscom817	yes	10.160.39.24
alidcscom151	alidcscom818	yes	10.160.39.25
alidcscom152	alidcscom819	no	10.160.39.80
alidcscom153	alidcscom820	yes	10.160.39.27

The server ‘alidcscom817’ (former ‘alidcscom150’) is dedicated for supervising the detector. The user interface of the SDD DCS is placed here. The PVSS system¹ on ‘alidcscom817’ is named ‘sdd_ui’.

On ‘alidcscom818’ (former ‘alidcscom151’) the low voltage supply, cooling and ventilation are controlled. The system ‘sdd_dcs’ is put here.

‘alidcscom819’ (former ‘alidcscom152’) controls the high voltage and is also utilized as the OPC server. The system on this computer is ‘sdd_infra’. At the

¹The ALICE DCS is distributed into several computers. This is possible because the PVSS structure is divided into, so called, systems. Each system has its name and may or may not communicate with other systems. For more information see [6].

present time (September 7, 2012) ‘alidcscom152’ is still being used because the high voltage is controlled via an interface plugged in a PCI bus but newer computers are equipped only with the PCI express buses. The full migration is being postponed until a PCI express – PCI reduction is added to ‘alidcscom819’.

‘alidcscom820’ (former ‘alidcscom153’) is a Linux machine, used as the DIM server of the SDD.

3.2 New FSM state BEAM_TUNING

The speed of the drifting electrons in the silicon drift detectors changes with the detectors’ temperature. The ALICE SDD utilizes a specific means of calibrating the drift speed [2, 16]. A number of electrodes have been installed on each detector in order to inject electrons into the detector, thus creating a charge that drifts towards the anode. By measuring the drift time it is possible to precisely calibrate the drift speed. These electrodes are called “MOS injectors” (see Fig. 3.1).

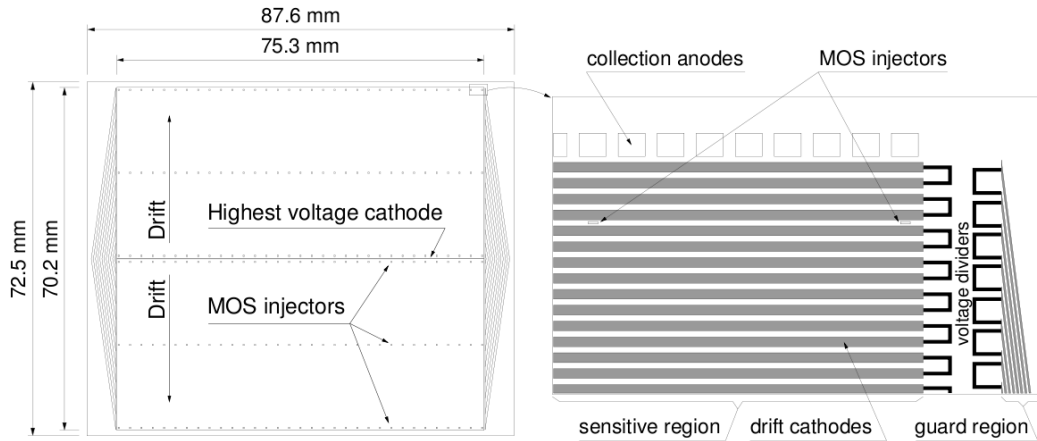


Figure 3.1: Layout of the Silicon Drift Detector [1].

In winter 2011 an accident happened to the SDD. A beam crashed near the ALICE detector when the SDD was in the **READY** state (i.e. with the high voltage on, with approximately 1.8 kV [4]), which led to destruction of almost a half of the MOS injectors.

To prevent similar events, a following step has been taken. A new state named **BEAM_TUNING** has been implemented. The voltage on all HV channels have been decreased to ≈ 100 V which should be a save value for the MOS injectors and other equipment of the detectors.

3.2.1 Ramping of high voltage

The **BEAM_TUNING** state, however useful, caused several problems. The HV channels sent too many error messages when going to ready, and also setting the detector to the **READY** state from **BEAM_TUNING** took too long.

The SDD employs HV supply (from the ISEG company) with some minor flaws. When the HV channels are set to a certain voltage, a slightly different voltage value is obtained. For this reason, a control script (on the computer `alidcscom152` by name `HV_auto.ct1`) has been implemented. This script is opened every 10 min and iteratively changes the set value of the voltage until it is within certain limits (0.1 V) from the desired voltage. This script had worked even before the `BEAM_TUNING` state was added.

When going to the `READY` state from `BEAM_TUNING` the system sent lots of error messages. After some investigation, we realized that this problem occurred because the HV supply somewhat overshoot the voltage. Therefore, the voltage value is now set at first on a slightly lower value (≈ 25 V less than the desired value).

Another problem was that the detector went to the `READY` state even though the voltage was not fully ramped. For this reason, the conditions of the `READY` state were changed so the SDD is not `READY` until the voltages are fully ramped up. This, however, caused that the SDD was not `READY` for 5 – 15 min after the `READY` state was triggered which was unacceptable.

To remove this inconvenience, several measures have been taken. A new control unit ‘`SddHvControl`’ have been added under the top (`Sdd`) unit, and the control script `HV_auto.ct1` was reedited so that it now works in two phases.

When the `READY` state is triggered, the SDD makes following tasks: `SddHvControl` goes to `FORCING` state in which the `HV_auto.ct1` script starts working in the first phase. In this phase the HV values are set within 1 V tolerance (the error messages are triggered when the voltages exceed 2 V limits); This takes ≈ 2 min. Then, the SDD goes `READY` and the `SddHvControl` goes to state `WORKING` which means that the control script does the second phase of adapting the voltages. In this state the voltages are set within 0.1 V tolerance. Then the `SddHvControl` goes `READY`.

Now, the waiting time for the SDD to go `READY` is approximately 2 min which is acceptable and the error messages were avoided as well. Moreover, because the `SddHvControl` was placed under the top unit, the system does not have to propagate the actions down to the HV channels, thus the load of the DCS computers is minimized.

3.3 Voltage control

When the low voltage supply is off for a longer period of time, it sometimes erases its settings. I.e. the set value in the PVSS is not downloaded to the power supply system. Hence, after every shutdown it is needed to reset the LV to its original settings. This had meant, before we implemented some improvements to the system, that every channel had had to be set manually. Moreover, there had not been a simple way for the operator to see if all the voltages had been set or not.

Therefore, a lot of effort has been made to improve the supervising of the low and high voltages, in the past year. The resetting of the voltages has been automatized and also several supervising tools have been added to the system.

3.3.1 Automation of setting voltages

A button that automatically sets all the low voltage channels to their right values have been added to the main control panel (see Fig. 3.2). A similar feature had already existed for the high voltage.

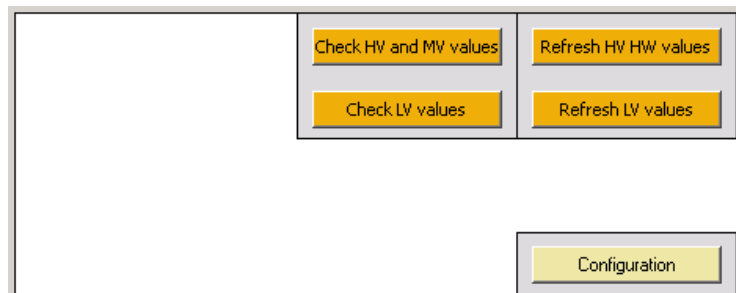


Figure 3.2: A view of a part of the main control panel: The buttons labeled “Refresh HV HW values” and “Refresh LV values” set the voltage values from PVSS to the voltage supply; The buttons labeled “Check HV and VM values” and “Check LV values” open the voltages summary described in subsection 3.3.2.

3.3.2 Improvements in supervising

When controlling such a complex detector as the SDD, it is needed to control all the voltage channels simultaneously, as well as one by one. It is possible to check the voltage channels individually. In the case of failure of only a part of the channels, however, it was not easy to find the faulty part of the detector. Therefore, some kind of summary of the voltages had to be implemented.

One of the measures, that have been taken, is a summary panel with colored squares that represent individual channels (see Fig. 3.3 for the low voltage, and 3.4 for the high voltage). For the HV and MV, the panel is logically divided into layers and modules, however the LV panel is composed of crates, boards and channels which makes the supervising easier because some of the LV channels are used by several modules.

Every square in the summary panel changes color, according to the voltage that is set in the power supply: green when the voltage in PVSS is set in the power supply; blue when the voltage in the power supply is not set at all (i.e. is set to zero), but the voltage in PVSS is set to a non-zero value; red when the value in the supply machine exceeds the value in PVSS; yellow if it is lower but not zero, and purple if the channel does not exist (see Fig. 3.5).

Another means of controlling the voltages is to write them into a text file. We have implemented a simple way that is accessible from the computer ‘alidcscom817’ (see section 3.1) from the ‘Start’ panel. The operator has only to type the path of the text file and click on the “Save” button. The text files are in the format easy to access via root or similar programs and are divided into three columns: channel number (crate/board/channel for the LV, and number of module, e.g. L3L04M5, for the MV and HV) — actual voltage (float) — set voltage (float) — is on (boolean

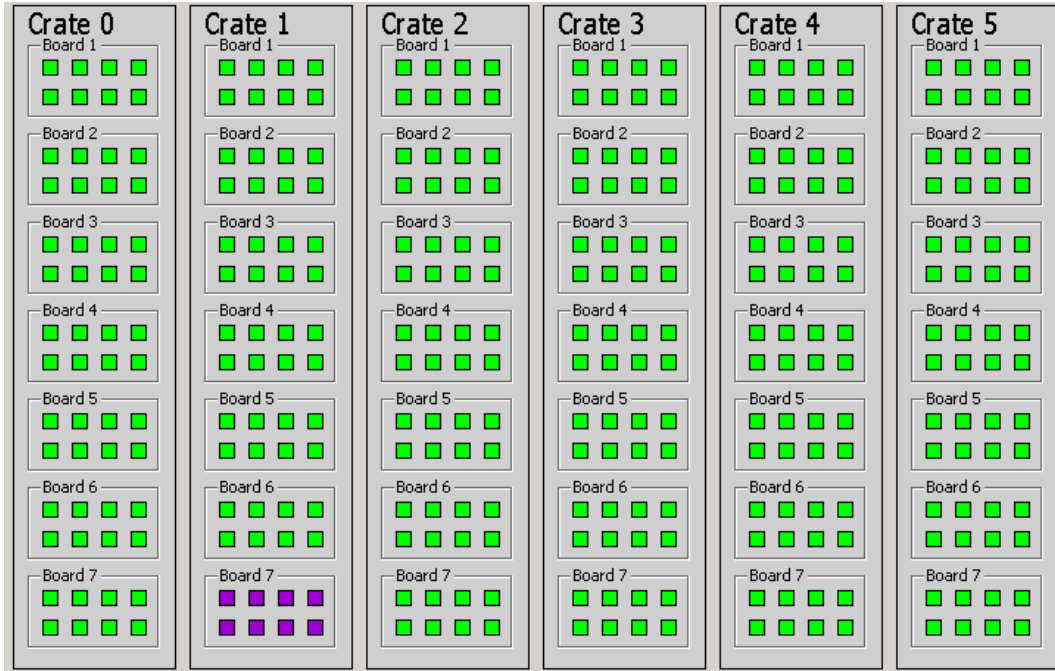


Figure 3.3: Panel for the low voltage summary.

value).

3.4 New humidity sensors

Two humidity sensors were installed on the SDD's C-side in the year 2011. The measured humidity values are accessible via datapoints that are located in the system 'dcs_globals' in a central DCS server. Therefore, to be able to perform supervising of humidity in the SDD, we needed to copy these datapoints to our system. We decided to copy them to the computer 'alidcscom817' (see section 3.1) in the system 'dcs_ui'. The names of the datapoints in the central DCS server and the copied datapoints in the server 'alidcscom817' are in Table 3.2.

Moreover, we put the humidity values into a trend plot so the user can easily check the change of humidity level in time. A picture of the humidity plot is in Fig. 3.6.

Table 3.2: Names of the datapoints copied from the system 'dcs_globals' on the central DCS server to the system 'sdd_ui' on the server 'alidcscom817'.

dcs_globals name	sdd_ui name
dcs_globals:aliEnv_humidity_SDD_C1_54	sdd_ui:humidity_SDD_C1_54
dcs_globals:aliEnv_humidity_SDD_C2_55	sdd_ui:humidity_SDD_C2_55

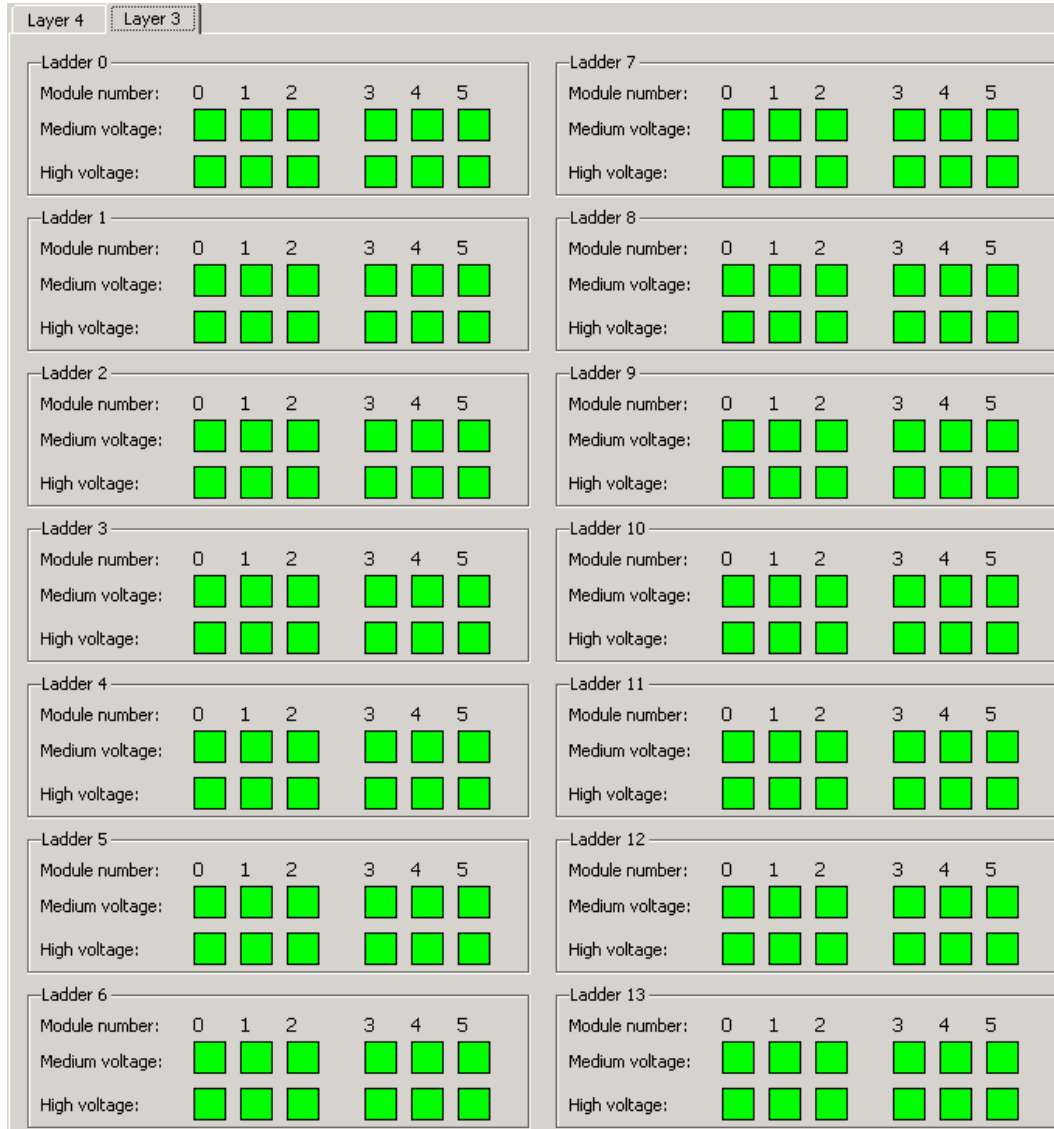


Figure 3.4: Panel for the high and medium voltage summary.

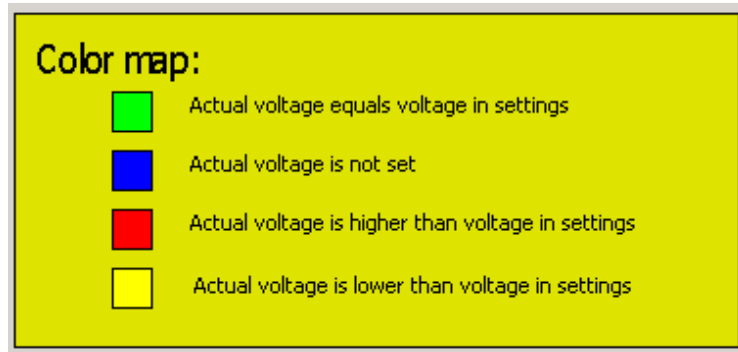


Figure 3.5: Color map of the voltage summaries.

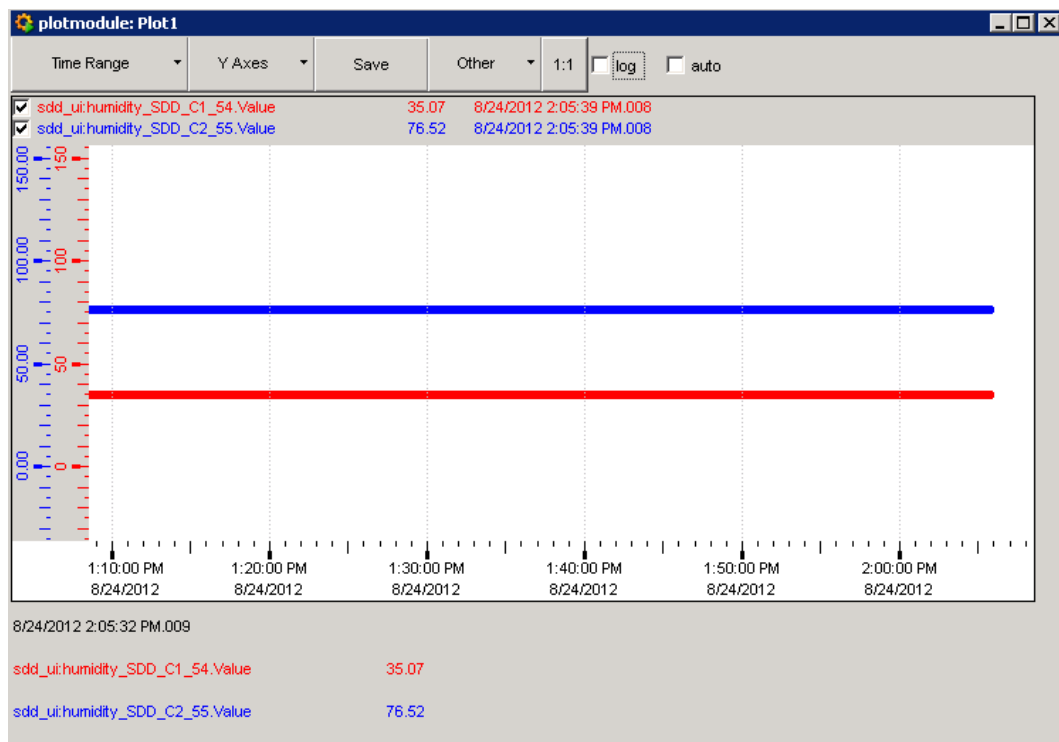


Figure 3.6: Humidity trend plot.

Chapter 4

Conclusion

The detector control system for the silicon drift detector is a complex and constantly evolving system. Several changes have been made to it in the past year (between September 2011 and August 2012).

The SDD DCS computers were subject to a major hardware upgrade. The SDD DCS servers have been migrated to new, more powerful, computers. Three machines out of four have been migrated, one server, however, still remains on an old computer because a PCI – PCI express reduction has to be added to the new server.

To protect the detectors in a period of time when no data is taken and the SDD still has to remain on, a new FSM state `BEAM_TUNING` has been implemented. In this state the high voltage channels are set to 100 V which is believed to be a safe value for the SDD, even when the SDD is put under huge amounts of radiation from misguided beams, etc.

When the `BEAM_TUNING` state was at first utilized, the SDD had suffered from some problems, when going to the `READY` state. A lot of errors concerning HV have occurred, and also the waiting time for `READY` was too long ($\approx 10 - 15$ min). Major changes to the FSM structure have been made to fix these problems, so that the errors have been avoided and the waiting time has decreased to ≈ 2 min.

Moreover, the voltages control has been significantly improved. All the voltage values on the LV channels can be set automatically at once, even after longer periods of time when they are off, which was not possible before.

The supervising of the voltages has experienced a lot of improvements as well. Panels with summaries of the voltage values were implemented so that the operators can now check all the voltages at once. Moreover, a new functionality, that allows the users to save all the voltage values instantly into a txt file easily readable by root programs, was added to the DCS.

Two humidity sensors were installed in the SDD space. Some supervising tools, including a trend plot, were developed to allow easier control of the humidity in SDD.

In this paper we have also documented the new structure of the FSM in SDD. What is more, the distribution of the various PVSS systems was documented here which has not been previously done.

List of Abbreviations

ACORDE	ALICE Cosmic Ray Detector
ACR	ALICE Control Room
ALICE	A Large Ion Collider Experiment
CaV	Cooling and Ventilation
CERN	Centre Européenne pour Recherche Nucléaire (European Organization for Nuclear Research)
CU	Control Unit
DAQ	Data Acquisition
DCS	Detector Control System
DIM	Distributed Information Management
DIP	Data Interchange Protocol
DP	DataPoint
DPT	DataPoint Type
DU	Device Units
ECS	Experiment Control System
EMCal	ElectroMagnetic CALorimeter
FERO	Front-End Electronics and Readout
FMD	Forward Multiplicity Detector
FSM	Finite State Machine
HLT	High-Level Trigger
HMPID	High Momentum Particle Identification Detector
HV	High Voltage

LIST OF ABBREVIATIONS

LEP	Large Electron-Positron Collider
LHC	Large Hadron Collider
LU	Logical Unit
LV	Low Voltage
MV	Medium Voltage
OPC	Object Linking and Embedding for Process Control
PHOS	Photon Spectrometer
PLC	Programmable Logic Controller
PMD	Photon Multiplicity Detector
PVSS	Prozessvisualierungs- und Steuerungs-System (Process Visualization and Control System)
QCD	Quantum ChromoDynamics
QGP	Quark-Gluon Plasma
SCADA	Supervisory Controls and Data Acquisition
SDD	Silicon Drift Detector
SPD	Silicon Pixel Detector
SSD	Silicon Strip Detector
T0	Time 0 detector
TOF	Time-of-Flight
TPC	Time-Projection Chamber
TRD	Transition Radiation Detector
TRG	Trigger System
UI	User Interface
V0	Vertex 0 detector
ZDC	Zero Degree Calorimeter

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