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Zprovoznění detektoru Muon Forward Tracker pro upgrade experimentu ALICE

Výzkumný úkol

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Vedoucí práce: prof. Jesús Guillermo Contreras Nuño, PhD.

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Czech Technical University in Prague
Faculty of Nuclear Sciences and Physical Engineering

II

Department of Physics

Commissioning of the Muon Forward Tracker for ALICE upgrade

Research project

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Originální zadání VU

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Diana Mária Krupová

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Diana Mária Krupová

Název práce:

Zprovoznění detektoru Muon Forward Tracker

pro upgrade experimentu ALICE

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Obor: Experimentální jaderná a částicová fyzika

Druh práce: Výzkumný úkol

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Abstrakt:

Muon Forward Tracker (MFT) představuje součást vylepšení systému detektorů ALICE během Long Shutdown 2 na LHC. MFT je nový detektor, který na detekci částic, stejně jako Inner Tracking System, využívá křemíkové ALPIDE senzory. Tato práce sa věnuje zprovoznění detektoru MFT. MFT se skládá z deset půl-disků, kterých základem je tzv. ladder, obsahující ALPIDE senzory. Práce popisuje postupy využívané na ohodnocení vlastností těchto součástí detektoru společně se statistickým zpracováním výsledků, čímž dospějeme k lepšímu porozumění chování detektoru.

Klíčová slova: CERN, ALICE, kremíkové detektory,
MFT, fyzika detektorov, LHC upgrade

Title:

Commissioning of the Muon Forward Tracker for ALICE upgrade

Author: Diana Mária Krupová

Field of study: Experimental Nuclear and Particle Physics

Thesis type: Research project

Supervisor: prof. Jesús Guillermo Contreras Nuño, PhD.

Abstract:

The Muon Forward Tracker (MFT) is being added to the ALICE detector system as a part of undergoing major upgrades during Long Shutdown 2 at the LHC. The MFT is a new tracking detector using the ALPIDE silicon chips common for the Inner Tracking System as the active detection element. This work is dedicated to the commissioning of the MFT. The MFT consists of 10 half-disks composed of ladders containing the ALPIDE sensors. The procedures used for qualification of the ladders are described along with quantitative analysis of the qualification results aiming at a better understanding of the detector performance.

Keywords: CERN, ALICE, silicon detectors,
MFT, detector physics, LHC upgrade

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Preface

One of the main objectives of high-energy physics (HEP) is to identify and to thoroughly describe the elementary constituents of matter as well as interactions among them, governed by the four fundamental forces. The Large Hadron Collider (LHC) at CERN together with all its detectors were built to provide new measurements towards this goal.

Currently, the LHC operation is interrupted in order to upgrade many of its components and to adapt for the planned operation with much higher luminosity. The ALICE detector is introduced in Chapter 1 along with prospects of its upgrade. In particular, a novel detector, the Muon Forward Tracker (MFT), was designed to improve the tracking capabilities of the ALICE detector system at forward rapidity.

The MFT is a silicon pixel detector. Chapter 2 contains the description of silicon properties—why it is suitable to use in HEP. The mechanism used to actually detect particles that pass the detector and to extract some information about the collision are described. The technology incorporated in ALPIDE chips is further presented in Chapter 3.

Chapter 4 includes the physics motivation to build the MFT and its layout. The detector uses a structure called *ladder*, where the ALPIDE chips are assembled. The characterisation of the ladders to ensure the quality of the MFT represents a part of the MFT commissioning presented in Chapter 5. The ladder qualification process was the main focus of my work at CERN. A statistical analysis for all the produced and tested ladders is summarised in Chapter 6. Finally, the conclusions and long-term outlook can be found in Chapter 7.

Chapter 1

The ALICE detector

The Standard Model (SM) represents the most successful theory of HEP. It has been tested countless of times in various experiments. Employing locally gauge-invariant quantum field theories, it combines the theory of the electroweak and the strong nuclear forces. Among the most impressive advances in understanding the SM and its consequences, an enormous progress has been made over the past years in the field of exploring a state of matter that we call the quark-gluon plasma (QGP). It is a medium described by quantum chromodynamics (QCD), characterised by a high temperature and density, where quarks are not confined in hadrons, instead they move across distances larger than the size of nucleons ($\sim$ 1 fm). A similar QCD medium existed in the early Universe, up to a few microseconds after the Big Bang [1].

To look into the world 10^{-15} times smaller than what we perceive in our lives, a large number of machines, devices and sophisticated tools is required. The advanced technology allows us to recreate the deconfined matter in a laboratory, or in a hadron collider, to be precise. With them we are able to reach the energies in the TeV range needed to explore the smallest distances. In this chapter two of such apparatus, the Large Hadron Collider and the ALICE detector, are described. A brief history of them is presented along with the prospects arriving with the current upgrade.

1.1 CERN and the LHC

The establishment of CERN (European Organization for Nuclear Research) was ratified in 1954 by the twelve founding member states [2]. CERN's first accelerator was the 600 MeV Synchrocyclotron. In 1959, the Proton Synchrotron (PS) was built as a new tool to study particle physics. The Super Proton Synchrotron (SPS) accelerated the first beam of protons in the 7-kilometre circular accelerator in 1976. The SPS was later converted to a $p\bar{p}$ collider and its two experiments UA1 and UA2 discovered the W and Z bosons, which led to the

1984 Nobel prize being awarded to Carlo Rubbia and Simon van der Meer *for their decisive contributions to the large project, which led to the discovery of the field particles W and Z, communicators of weak interaction* [3]. A new era came with the excavation of the 27-kilometre tunnel where the Large Electron-Positron (LEP) collider was built. The LEP with 5176 magnets and 128 accelerating cavities installed [2] was commissioned in 1989. The LEP accelerator operated at energies in the 100-200 GeV range. LEP provided a detailed study of the electroweak interaction.

After Rubbia's idea [4] of dismissing the Large Electron-Positron (LEP) collider in favour of a hadron collider and to reach the desired ultra-high beam energies, the 27-kilometre tunnel was adjusted to be capable of colliding hadrons, which required for example developing the large superconducting magnets in addition to all the other improvements. That is how the Large Hadron Collider (LHC) was born — after a few years of building and preparation, it first started operations on September 10, 2008. The first LHC run[1] (Run 1), however, was delayed due to an incident and did not start until the end of 2009. After the Long Shutdown 1 (LS1, 2013-2015) upgrade, the second operational LHC run (Run 2) started in 2015 and also lasted for three years. Currently, we are in the period of the Long Shutdown 2 (LS2), which was recently extended up until 2021.

The four main experiments at the LHC are:

- ALICE, further described in Section 1.2,
- LHCb (Large Hadron Collider beauty), specialising in the differences between matter and antimatter by studying the b quark,
- ATLAS and CMS, general-purpose detectors investigating a wide range of physics. While deeply studying the Standard Model, the Higgs boson has been discovered in 2012 by both the ATLAS [5] and CMS [6] collaborations[2].

During the LHC Run 2, the protons were accelerated to $\sqrt{s} = 13$ TeV for pp collisions. Few months of the run were dedicated to heavy-ion physics, colliding lead ions (^{208}Pb) on either p–Pb (reaching $\sqrt{s_{\mathrm{pN}}} = 8.16$ TeV) or Pb–Pb collisions (at $\sqrt{s_{\mathrm{NN}}} = 5.02$ TeV) [8]. A similar schedule is planned for Run 3.

[1] LHC operates in three-year periods called *runs* according to a schedule that is planned for up to twenty years ahead.

[2] The Higgs boson discovery contributed to the 2013 Nobel prize in physics that was awarded jointly to François Englert and Peter W. Higgs *for the theoretical discovery of a mechanism that contributes to our understanding of the origin of mass of subatomic particles, and which recently was confirmed through the discovery of the predicted fundamental particle, by the ATLAS and CMS experiments at CERN's Large Hadron Collider* [7].

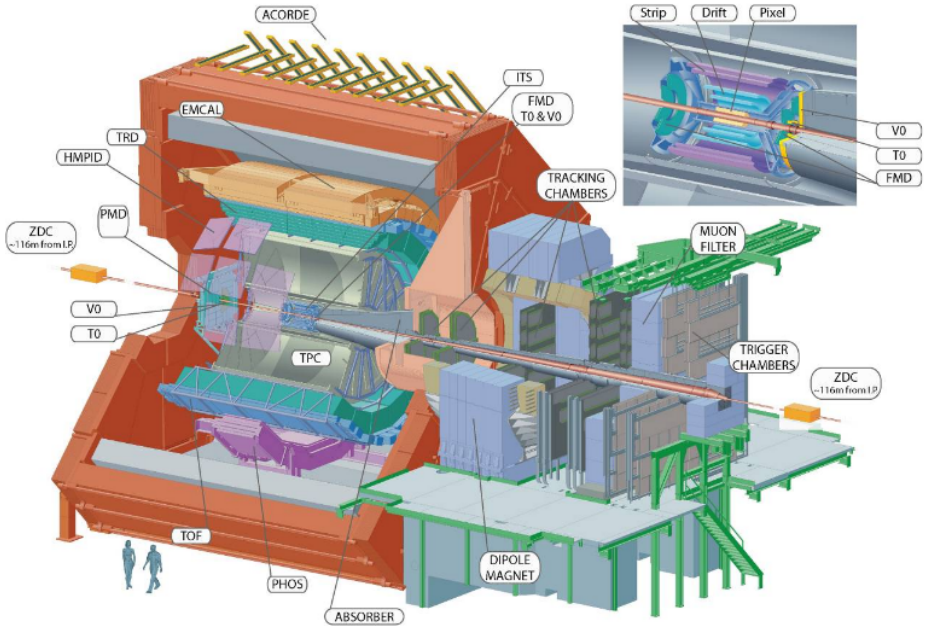


Fig. 1.1: The layout of the ALICE detector with all the sub-detectors labelled with their acronyms. Taken from [9].

1.2 A Large Ion Collider Experiment

ALICE, standing for *A Large Ion Collider Experiment*, is somehow different from the other experiments at the LHC - its main purpose is the study of head-on heavy-ion collisions. The detector has to measure a plethora of escaping particles originating in the collision to reconstruct their number, mass, type or energy.

The search for the QGP originated in 1986 at the SPS and Brookhaven AGS (Alternating Gradient Synchrotron) simultaneously. Later - in 1987 and 1990 respectively, it was decided that the LHC would collide heavy ions as well as protons and the RHIC (Relativistic Heavy Ion Collider) was approved. The R&D effort for a large general purpose heavy-ion detector at the LHC started immediately. One of the challenges was to achieve good resolution at both high and low momentum - with a large dynamic range required for momentum measurement, ranging from tens of MeV to over 100 GeV [9]. The technical proposal for the ALICE was approved in 1997.

During the LHC Run 1, the experiment consisted of 17 different detection systems [9]; each of them with different technology choice and specific method of detecting particles. A schematic view of ALICE is shown in Fig. 1.1. The central barrel, containing the tracking detectors and covering the pseudorapidity $-0.9 < \eta < 0.9$, is located inside a solenoid magnet. The magnet, originally

built for LEP in the 1980's, creates a magnetic field of 0.5 T parallel to the beam line. The momenta of the charged particles are given by the curvature of their path inside the magnetic field. A set of particle identification (PID) detectors is employed at ALICE using all known PID techniques. Two types of electromagnetic calorimeters (EMCal) are used for photon and jet measurements. The forward muon arm with the Muon Spectrometer (MS) covers the pseudorapidity $-4.0 < \eta < -2.5$.

ALICE uses the following coordinate reference system [10]:

- the z-axis on the beam line, positive z-axis pointing in the direction opposite to the muon spectrometer,
- the x-axis on the LHC horizontal plane, pointing to the centre of the accelerator,
- the y-axis pointing upwards,
- the cylindrical coordinates r and ϕ in the transverse plane localising the radial coordinate of the point with respect to the centre of axis, azimuthal angle measured from x to y.

1.2.1 ALICE subdetectors

- **Inner Tracking System**

  The Inner Tracking System (ITS) aims at identifying and localising the primary vertices with μm accuracy and reconstructing the secondary vertices originating from the decays of unstable particles.

  ITS consists of three parts, each with two layers (see Fig. 1.2):

  - silicon pixel detector (SPD) - innermost layers,
  - silicon drift detector (SDD) - middle layers,
  - silicon strip detector (SSD) - outermost layers.

  The ITS is also upgraded during LS2 - see Section 1.3.2.

- **Time Projection Chamber**

  The Time Projection Chamber (TPC) is the *queen* of all gaseous detectors. It serves as the main tracking detector at central rapidites.

  The TPC provides three-dimensional (3D) information for tracking and momentum measurement together with PID via the measurement of the specific energy loss. It is the only electronically read gaseous detector delivering direct 3D track information: for each point on the track, x, y and z coordinates are measured simultaneously.

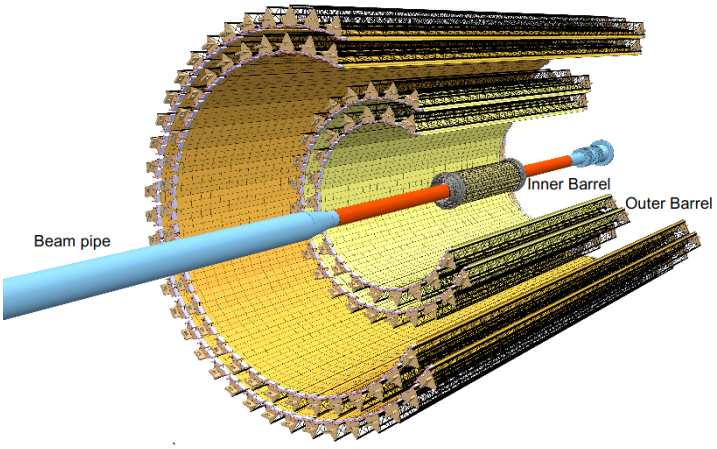


Fig. 1.2: Layout of the ITS detector. Taken from [11].

The TPC at ALICE consists of a double cylinder around the beam pipe, 5 m long, centered on the IP and inside the solenoid magnet [12]. The overall dimensions of the TPC together with the segmentation of the read-out planes will remain unchanged after the upgrade.

The upgraded TPC will be operated with a Ne-CO_2-N_2 (90-10-5) gas mixture, as the ion mobility in neon is higher compared to argon, leading to less space-charge accumulation in the drift field of 400 V/cm [13]. The currently employed multi-wire proportional chambers (MWPC) will be replaced by the GEM-based (gas electron multiplier) read-out chambers.

- **Transition Radiation Detectors**

  Highly relativistic particles (Lorentz factor $\gamma \gg 1$) emit photons when crossing from a medium with one dielectric constant into another. While the emission probability for such photons is small, its conversion leads to a large energy deposit compared to the average energy deposit via ionisation.

  The fact that the total energy loss by a charged particle is proportional to the Lorentz factor of a particle but inversely proportional to the angle of emission of transition radiation (TR) photons leads to the application of transition radiation for particle identification at high momenta.

  The γ-dependent effect of TR is extremely valuable for PID at high energies. There is a wide momentum range (1–100 GeV/c) where electrons (or positrons) are the only particles producing transition radiation, which can be used for the separation of the electrons from kaons or pions. Therefore, transition radiation detectors in general are mainly used to identify electrons.

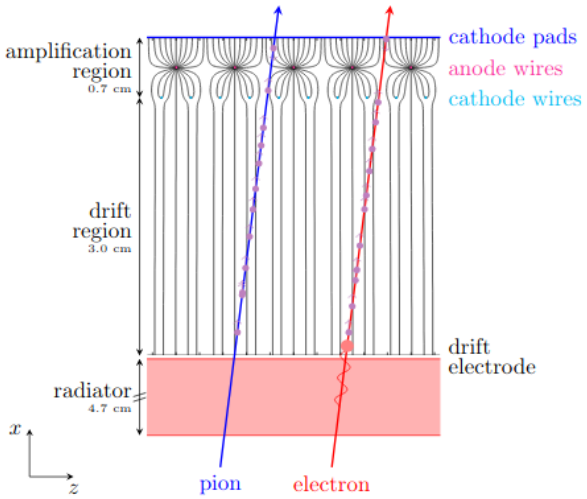


Fig. 1.3: Schematic cross-section of a TRD chamber in the $x-z$ plane. Taken from [14].

The ALICE Transition Radiaton Detector (TRD) uses MWPCs as a basic component. Fig. 1.3 shows the tracks of a pion and an electron to illustrate the ionisation energy deposition and the TR contribution. The drift lines are represented by the solid lines. The ALICE TRD uses a thick radiator, which is not drawn to scale in the figure. The radiator is mounted in front of the drift section. The TR photons are produced in the radiator and then absorbed in a Xe-based gas mixture. An eighteen-fold segmentation [14] in azimuth ϕ was chosen to match the TPC read-out chambers.

- **Time-of-Flight Detector**

  In ALICE, the main purpose of the Time-of-Flight (ToF) detector is the PID in a large part of the phase space. The ToF detector uses an array of multi-resistive plate chambers (MRPCs) covering a cylindrical surface around the IP. A ToF measurement is one of the methods to obtain the particle velocity. The velocity then serves for the PID: when the momentum is measured simultaneously, it is possible to reconstruct the charge and mass of the produced hadrons.

  The ToF detector measures the stopping time, while the collision time is measured with extreme precision ($\sim$ 25 ps at high multiplicities) by two sets of twelve Cherenkov counters T0 mounted tightly around the beam pipe.

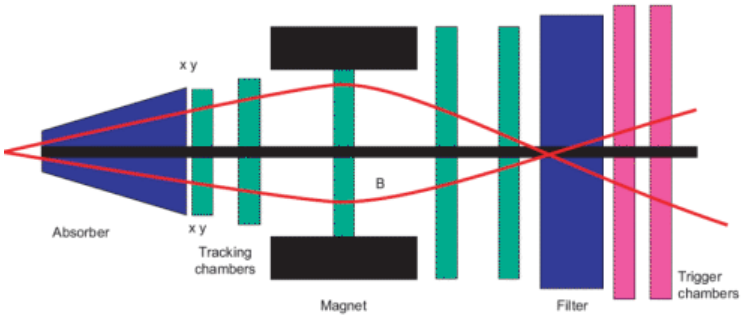


Fig. 1.4: A longitudinal cross section view of the ALICE MS. Taken from [16].

- **Muon Spectrometer**

  The ALICE Muon Spectrometer [15] is designed to study open heavy flavour and quarkonia production via their dimuon ($\mu^+\mu^-$) decay channel.

  The schematic cross section of the spectrometer is shown in Fig. 1.4.

  The spectrometer consists of:

  – the front absorber to absorb hadrons and photons from the interaction vertex; the absorber is made out of carbon, steel, tungsten and concrete, located inside the solenoid magnet, weighs 50 tons and is 4.13 m long,

  – high-granularity tracking system of 10 detection planes,

  – a 3 Tm dipole magnet,

  – muon filter wall, followed by trigger chambers,

  – inner beam shield to protect the chambers from primary and secondary particles produced at large rapidities.

  For tracking, the muon spectrometer uses cathode pad chambers to achieve space resolution of 100 μm. The pad chambers are organised in five stations composed of two planes in order to get two-dimensional position information.

  Four planes of 18 resistive plate chambers (RPCs) are used in the trigger chambers. The chambers are arranged in two stations and cover a total surface of 140 m^2.

- **Zero Degree Calorimeter**

  The ALICE Zero Degree Calorimeter (ZDC) [17] consists of two sets of small, very compact calorimeters, each of which is located on one side, more than 100 m from the IP along the beam pipe. The measurement

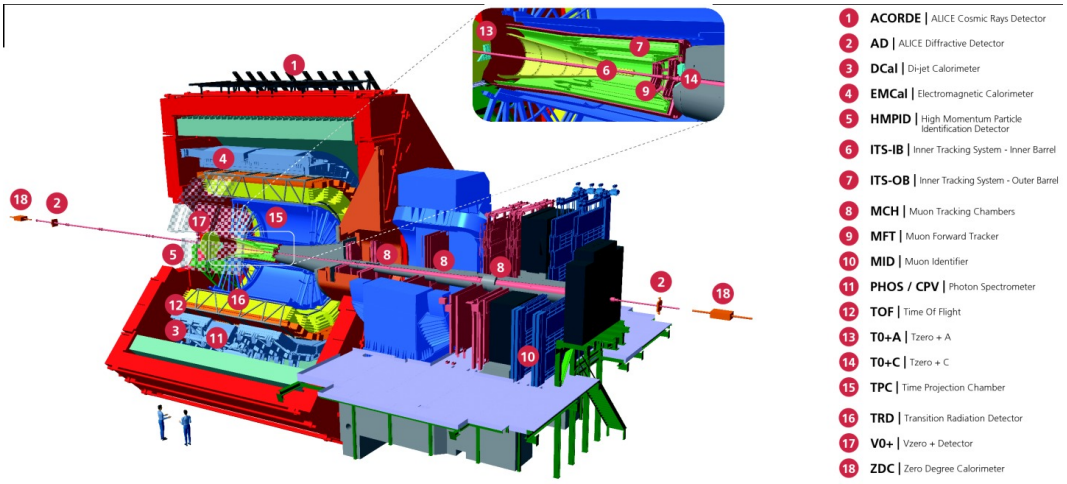


Fig. 1.5: ALICE detector in Run 3 configuration - after the upgrade. Taken from [19].

of energy carried away by the spectator nucleons from the heavy-ion collision in the forward direction is performed by the ZDC.

- **V0 detector**

  The V0 detector [18] consists of two arrays of scintillator counters used to select interactions and to reject beam related background events.

1.3 ALICE upgrade plans

The ALICE experiment will be upgraded during the Long Shutdown 2 (LS2) in order to exploit to the fullest the scientific potential of the future LHC. The ALICE layout together with all the detection systems after the upgrade can be seen in Fig. 1.5. The upgrade during LS2 includes [20]:

- a smaller diameter beam pipe;
- ITS upgrade, further described in Section 1.3.2;
- MFT, see Chapter 4;
- TPC upgrade, the replacement of the wire chambers with GEM detectors and new pipelined read-out electronics;
- read-out electronics upgrade of the TRD, ToF detector and Muon Spectrometer to achieve higher operation rate;
- upgrade of the forward trigger detectors;

- upgrade of the online systems and offline reconstruction and an analysis framework.

After the LS2, the LHC will provide Pb–Pb collisions at an interaction rate of up to 50 kHz, corresponding to an instantaneous luminosity $\mathcal{L} = 6 \times 10^{27}$ cm^{-2} s^{-1} [10]. The upgrade strategy of ALICE is taking that into account and designed all of its upgrade plans in a way to be able to process such a big rate; that means to improve tracking and vertexing capabilities, radiation hardness and first of all, to be able to accumulate enough statistics for the upgrade physics program.

1.3.1 Upgrade of computing system

ALICE needs to integrate a luminosity of 13 nb^{-1} for minimum bias Pb–Pb collisions together with dedicated p–Pb and pp reference runs.

The necessity to upgrade the computing system will be illustrated with the TPC, the largest contributor to the data volume.

In order to keep up with the 50 kHz interaction rate, the TPC will require the implementation of a continuous read-out process to deal with event pile-up and avoid trigger-generated dead time. Compared to Runs 1 and 2, this is significantly more challenging for the online and offline computing systems.

The resulting data throughput from the detector has been estimated to be larger than 1 TB/s for Pb–Pb events, two orders of magnitude more than in Run 1.

The zero-suppressed data of all collisions will be shipped to the O^2 (Online-Offline computing system) [21] facility at the anticipated interaction rate of 50 kHz for Pb–Pb collisions or 200 kHz for pp and p–Pb collisions.

The raw data of the TPC will first be rapidly reconstructed using online cluster finding and a first fast tracking using an early calibration based on average running conditions. Data produced during this stage will be stored temporarily. taking advantage of the duty factor of the accelerator and the experiment, the second reconstruction stage will be performed asynchronously, using the final calibration in order to reach the required data quality.

The O^2 facility will be sufficient to perform both the synchronous fast reconstruction and asynchronous reconstruction during data taking.

1.3.2 ITS upgrade

As far as the physics performance in heavy flavour detection is concerned, the current ITS has significant limitations [10]. A separation of the secondary vertices produced by the decay of charm baryons is not possible, as the impact parameter resolution of the ITS is larger than the decay length of Λ_c baryon: 60 μm. Therefore, the study of charm baryons with the current detector is not optimal.

As mentioned before, the radius of the beam pipe will get reduced (29.0 mm $\rightarrow$ 17.2 mm) during LS2. For a tracking detector to reach an optimal performance, it should be placed as close to the IP as possible, as many particles of interest live for a very short time τ before decaying into daughter particles.

Fig. 1.6 shows the schematic layout of the new ITS. A grouping of the seven layers in two separate barrels is provided. The three innermost layers form the Inner Barrel, while the four outermost layers compose the Outer Barrel. The ITS layers are azimuthally segmented in units named staves. The staves serve as an equivalent of the ladder structures used in the MFT and are mechanically independent.

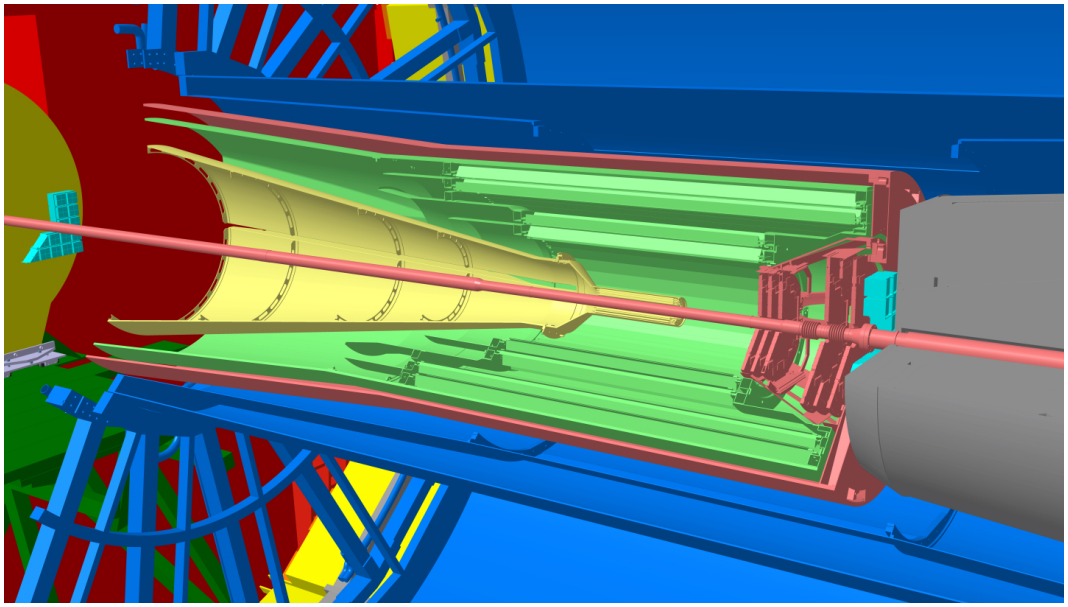


Fig. 1.6: ITS schematic layout including the MFT for Run 3. Taken from [22].

The spatial resolution for upgraded ITS [11] will get improved by a factor of 3 as a result of

1. placing the first layer of the new ITS detector closer to the beam pipe,
2. the reduction of the material budget per layer,

3. geometry and segmentation: a reduced pixel size from 50 μm $\times$ 425 μm to 30$\times$30 μm^2 with a thickness of 50 μm.

To reduce the material budget and improve the granularity of the detector system, both read-out and sensor are implemented on a single silicon substrate. This approach led to the development of CMOS Monolithic Active Pixel Sensors (MAPS), also used for the MFT detector (see Chapter 3).

The read-out time featured before LS2 was 1 kHz. The new ITS detector is designed to be able to read the data from each of the individual interactions up to a rate of 100 kHz for Pb–Pb collisions and 400 kHz for pp collisions, two times higher than the ALICE upgrade requirements.

The accessibility for the ITS system will also get implemented during LS2: the efficient insertion and removal of the detector parts during the yearly LHC shutdowns will majorly improve.

Chapter 2

Silicon detectors in high-energy physics

Silicon detectors are widely used for many applications. Historically, they have enabled economically reasonable fiber-based optical communication, optical storage, high-frequency amplification and revolutionised technological developments of everyday life: photography, display technology or lighting. Their properties, low price and potential for numerous applications made them widely used in HEP as an easy way to detect and to extract some information about the particles.

The main detection element of the MFT, the focus of this work, is a semiconductor (silicon) sensor. In this chapter, we draw a picture of how semiconductor detectors work.

2.1 Silicon properties

Reasons to use silicon (Si) as a semiconductor sensor spring from its properties [23]:

- an abundant element - 26% of the Earth crust,
- relatively easy and cheap to grow it in large crystals of very high purity,
- easy to modify electrical properties of silicon in a process called doping - introducing atoms of other chemical elements in the crystal lattice,
- wide range of temperatures for operation (-55°C to 125°C),
- easy formation of oxide - SiO_2 which behaves as an almost ideal insulator,
- excellent thermal and mechanical properties.

More properties are summarised in Table 2.1.

atomic number	14
atomic weight	28.0855
electron distribution per shell	2, 8, 4
density	2.33 g·cm^{-3}
melting point	1414 °C
band gap energy at 300 K	1.12 eV
intrinsic carrier concentration	1.45·10^{10} cm^{-3}
electron mobility	1500 cm^2/V·s
hole mobility	500 cm^2/V·s

Table 2.1: Fundamental properties of silicon, values taken from [23].

2.1.1 Silicon band structure

The semiconductor properties of silicon originate from its band structure, see Fig. 2.1. Electrons involved in bonds between atoms occupy states in the valence band and they are localised in the proximity of the atoms. Electrons in the conduction band are not attached to any atom and they can easily move through the crystal under an electric field. The two bands are separated by an energy gap of 1.12 eV with no accessible states present.

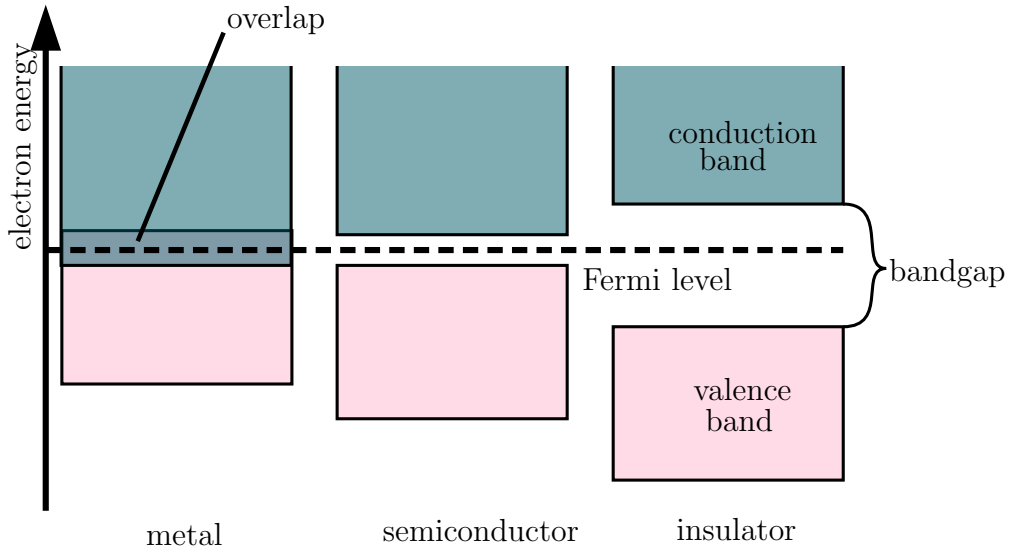


Fig. 2.1: A diagram comparing the electron band structures of metals, semiconductors and insulators.

At low temperatures near absolute zero, all the states in the valence band are occupied and all the states in the conduction band are empty. Therefore, no free carriers are available for conduction and the material behaves as an

insulator. With the temperature rising, electrons acquire thermal energy until they make a transition into the conduction band. The electron leaves behind an empty location in the valence band, known as a *hole*. Electrons and holes can also recombine.

Doping

The introduction of impurities into semiconductors is called *doping* [24]. Doping allows to change of the concentration of electrons and holes in silicon.

Various methods of doping are used, a straightforward method of doping is the incorporation during crystal growth or epitaxy.

In the process of doping, atoms with either three or five electrons in outer shell are introduced into the silicon crystal lattice.

If the foreign atom has three electrons in its outer shell, it forms three bonds with silicon producing a vacancy in the lattice that serves as a charge carrier and which an electron from a nearby silicon atom can fill. We call the silicon doped with acceptor atoms (mostly trivalent boron, B) the p-type. The opposite situation is created by using pentavalent donor atoms (mostly phosphorus, P) for doping. The donor forms four bonds with silicon while losing one electron, therefore becomes positively charged. This process creates the n-type silicon.

2.2 Interaction of particles with matter

The interaction of particles with matter depends on both the incoming type of radiation, as well as the energy. Detectors used in high energy experiments need to be designed in a way to capture all types of interactions. A wide range of subdetectors, each made for a specific task, is used to catch the flow of large amount of data and also to choose what we need.

A process referred to as *energy-loss process*, where the energy of a particle is dissipated inside a material, is caused by the interaction of the electric field of the particle to be detected with the one generated by the (either electronic or even nuclear) structure of the detecting medium.

2.2.1 Energy loss of charged particles

Any type of moving charged particle inside matter will lose energy. The collision process induced by massive charged particles[1], mainly caused by elastic collisions with electrons, was studied by many physicists of the beginning of

[1]By *massive* charged particles we call the particles with rest mass much larger than the rest mass of electron, $m_e = 511$ keV.

the 20th century. Bethe (1930) was among the first to study the energy loss in quantum mechanics, Bloch (1933) later added the relativistic corrections.

For an incoming particle of velocity $v = \beta c$ and charge number z, the theoretical expression for the energy loss by collision[2] $\frac{\mathrm{d}E}{\mathrm{d}x}$ (in a form containing corrections for density and shell effects) is called the Bethe-Bloch formula [25]:

$$\frac{\mathrm{d}E}{\mathrm{d}x} = 2\pi N_0 r_\mathrm{e}^2 m_\mathrm{e} c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[\ln\left(\frac{2m_\mathrm{e}\gamma^2 v^2 W_\mathrm{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right], \qquad (2.1)$$

where m_e is the electron mass, $r_e = \frac{e^2}{4\pi m_e c^2}$ is the classical electron radius, $N_0 = 6.022 \cdot 10^{23}$ is Avogadro's number, I is the effective ionisation potential averaged over all electrons, Z, A are the atomic number and atomic weight of the medium, ρ is the density of medium, $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ is the Lorentz relativistic factor, δ is a density correction, C is a shell correction and W_max is the maximum energy transfer in a single collision. The shell correction C is important at very low velocity and the density correction δ flattens the relativistic rise.

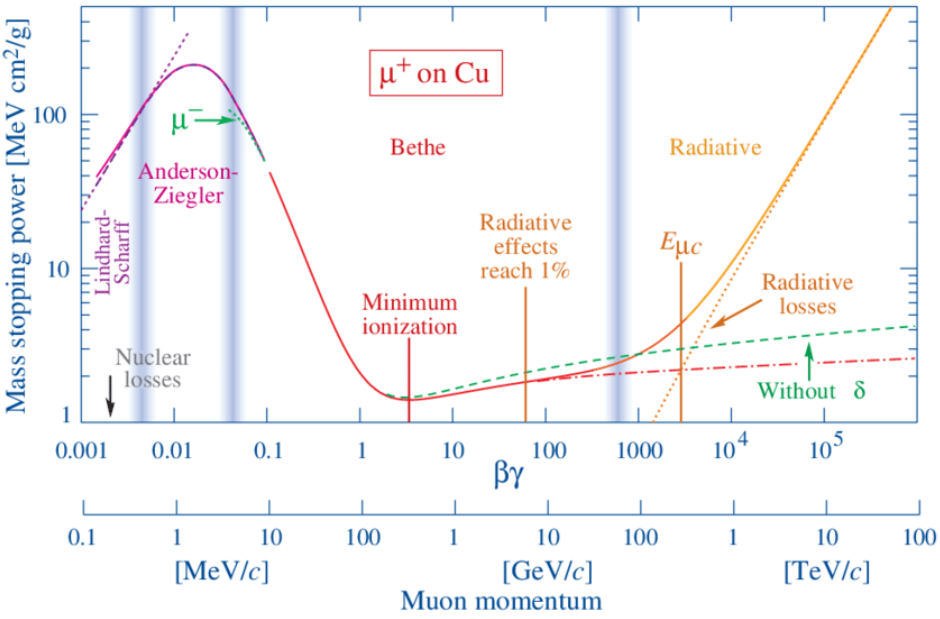


Fig. 2.2: Stopping power of muons in copper. Taken from [26].

The Bethe-Bloch formula with corrrections is illustrated in Fig. 2.2 for positively charged muons on copper.

In the Bethe-Bloch formula, we only considered phenomena related to the energy released electromagnetically by charged particle. However, there are

[2] also reffered to as the stopping power

additional effects in energy loss. When a charged particle passes in the neighbourhood of a nucleus, the most important effect is the deflection of its trajectory [27], associated with the emission of photons. We approximate the phenomenon with elastic Coulomb scattering.

The incident particle of charge ze acquires an equal, but opposite transverse momentum with respect to the one acquired by the recoil nucleus of charge Ze. This transferred momentum is very small in comparison with the incoming particle momentum p. The scattering angle θ is given approximately by the ratio of the transverse momentum to the total momentum p, i.e.

$$\theta = \frac{2Zze^2}{bvp}, \tag{2.2}$$

where v is the particle velocity.

2.2.2 Energy loss of electromagnetic radiaton

Electromagnetic radiation interacts with detectors mainly via three processes: the photoelectric effect, the Compton effect and pair production. The incident radiation is either completely absorbed in the sensor material (photoelectric effect, pair production) or is scattered to relatively large angles (Compton).

A monochromatic photon beam traversing the sensor material is not modified in energy but attenuated in intensity

$$I(x) = I_0 e^{-x/\lambda}, \tag{2.3}$$

where I_0 and $I(x)$ are the beam intensity before and after traversing a material of thickness x, respectively. The λ denotes the attenuation length, a property of the medium depending also on the photon energy.

At low energies (below 100 keV for silicon), the photoelectric effect dominates. With larger energies, the scattering and pair production become dominant. Silicon is mostly used for photon detection up to energies about 100 keV [25].

2.3 The p-n diode junction

The p-n diode junction (Fig. 2.3) is very basic but one of the most important electronic structures. It can be used a particle detector: a traversing particle, i.e. produced in a collision, generates electron-hole pairs in the depletion zone, which creates a charge signal.

The p-n junction is obtained by joining a p-type with a n-type extrinsic semiconductor together.

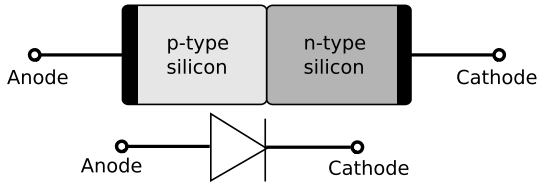


Fig. 2.3: A p-n diode structure and device schematic [28].

While the p-type and n-type regions in the junction are separated in thermal equilibrium, the charge carriers, that is the electrons and holes are homogeneously distributed in their volumes. Bringing the two parts into contact sets off a diffusion process of electrons into the p-type region and holes into the n-type region. A surplus of negative charge in the p-type region (positive charge in the n-type region) is created which generates an electric field counteracting the diffusion. Therefore, a region of non-mobile space charge is formed. The potential barrier V_{bi} is generated between the two space charge densities, preventing electrons and holes from diffusing further. The situation is illustrated in Fig. 2.4. No mobile charge carrier is present in the central zone of the junction - the depletion zone: a region in either side at the junction, which does not contain any mobile charge carriers. It plays an important role in the physics of the MOS transistor.

2.3.1 Silicon p-n junction as a sensor

When an ionising particle traverses the depletion zone in the p-n junction, it deposits a fraction of its energy, the mean value of the energy loss is described by Eq. 2.1. The electron-hole pairs, created in the depletion region, drift under the influence of the electric field giving rise to a current.

An external voltage can be applied to a p-n junctions in two ways: in forward bias and reverse bias, also called back bias. In a forward bias scenario, i.e. the positive terminal of a source is connected to the p-type side and the negative terminal of a source is connected to the n-type side, the voltage across the junction decreases from the equilibrium value V_{bi} by the externally applied positive voltage V to $V_{\mathrm{bi}} - V$ which shrinks the width of the depletion region.

If the diode is back biased, i.e. the positive terminal of a source is connected to the n-type side and the negative terminal of a source is connected to the p-type side, the depletion region becomes wider with increasing back bias voltage until a certain value of voltage, when the depletion region gets destroyed and a reverse current starts to flow through the diode.

The current-voltage (I-V) characteristics (see Fig. 2.5) illustrates the described behaviour of a p-n diode. The voltage that is conducting current in forward bias direction (denoted V_{d} in Fig. 2.5) is typically in order of 1 V -

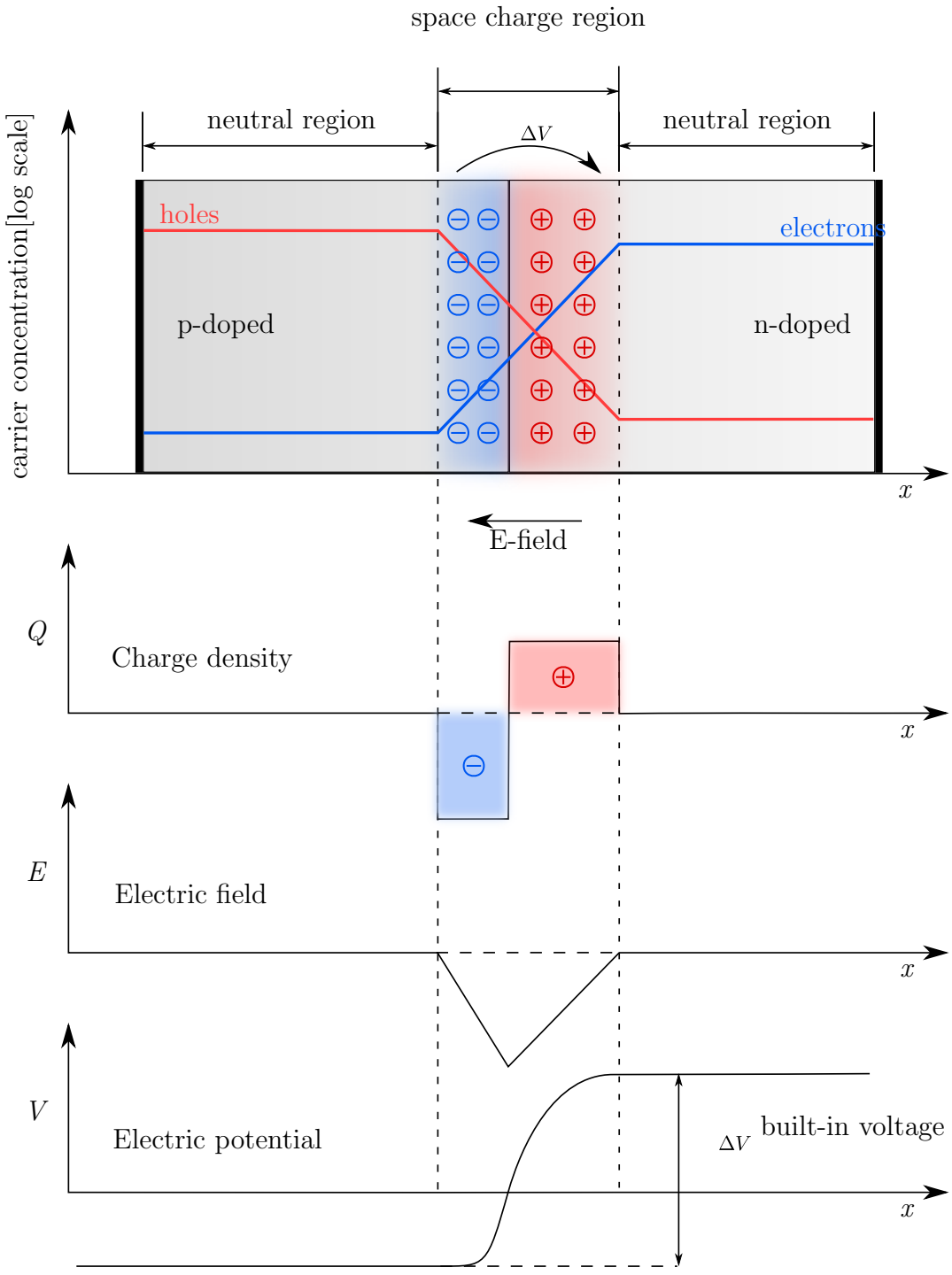


Fig. 2.4: Approximation of charge density Q, electric field E and electric potential V [29].

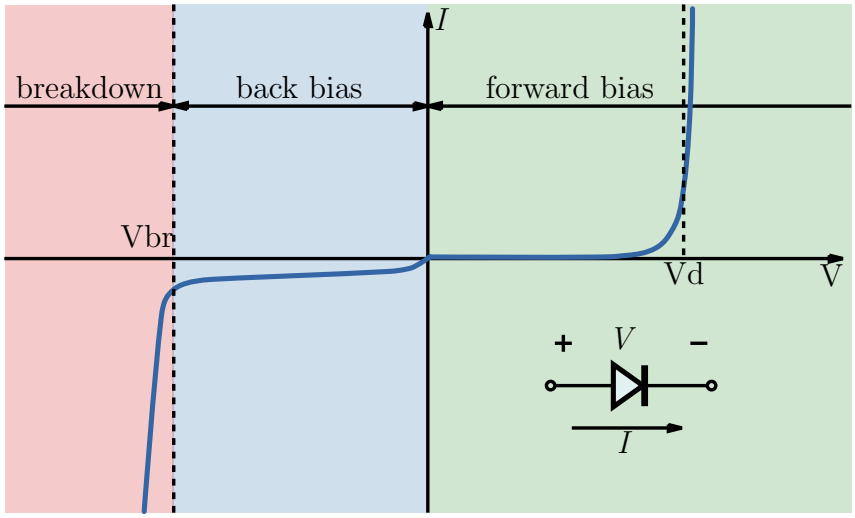


Fig. 2.5: The current-voltage characteristics of a p-n junction.

for a silicon diode, it is 0.7 V, while typical values for breakdown voltage V_{br} are ~ 10 V.

ALPIDE chips can be be operated with back bias voltage V_{bb}. In order to perform the qualification tests (see Chapter 5), two configurations are used: $V_{\mathrm{bb}} = 0$ V and $V_{\mathrm{bb}} = -3$ V.

2.3.2 Types of silicon detectors

One subcategory of silicon detectors are those that can only be used for energy, not for position measurement. These include the simple unbiased diode or the back-biased diode. On the other hand, position-sensitive detectors may also measure energy; perhaps with even higher precision, as most semiconductor detectors will provide the energy measurement if the read-out electronics measures the signal charge. The position sensitivity may be obtained by the segmentation into large number of small subdetectors that are read out separately or by dividing the created charge into few read-out electrodes, where the ratio of charges depends on where the charge was created.

2.4 CMOS technology

Complementary metal-oxide-semiconductor (CMOS) [23] is a type of MOSFET (metal-oxide-semiconductor field effect transistor) fabrication process allowing the fabrication of integrated circuits containing complementary and symmetrical pairs of p-type and n-type MOSFETs, thus creating elements for logic functions, widely used in microelectronics.

The monolithic silicon pixel chip developed for the ITS and the MFT, ALPIDE, is implemented in the 180 nm CMOS technology.

2.4.1 MOSFET

Besides a p-n junction diode, the transistor is another very important semiconductor device used to amplify or switch electronic signals and electrical power. Transistors in general are classified into unipolar and bipolar, each with completely different operating principles. Bipolar transistors are mostly used as amplifiers and switches. Unipolar transistors are more common in digital circuitry - MOSFETs.

In an era of vaccuum tubes widely used in technology, just two days before Christmas in 1947, the inventors of the transistors[3] constructed a tiny amplifier on a chunk of germanium. As [30] depicts, they could envision a time when there would be no more vacuum tubes, no more high voltage supplies, no more power wasted in heating elements. The world could look forward to the first microcomputer, the Walkman, and then the boom-box: the amazingly tiny microcircuit housed in the amazingly huge suitcase.

The basic idea beyond the MOS transistor is that one electrode, the **gate**, controls through capacitive coupling the conductivity between other two electrodes, called **drain** and **source**. The transistor behaves like a switch that establishes or prevents an electrical contact between two points in a circuit. The use of MOS transistor as a switch is the basis for digital circuits.

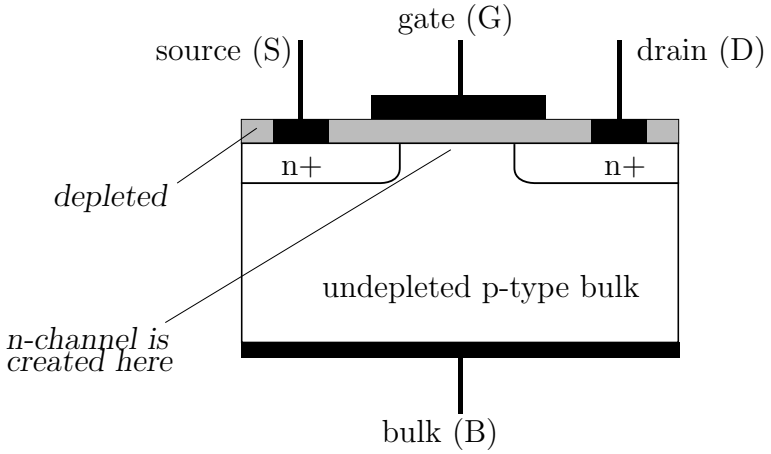


Fig. 2.6: A cross section typical for an n-channel MOSFET.

The MOSFET cross section is shown in Fig. 2.6. The driving electrodes are the gate and substrate (bulk), the output electrodes are the drain and source.

[3] John Bardeen and Walter Brattain, both of whom worked at Bell labs.

While a bipolar transistor is conducted by the input (emitter to base) current, a MOSFET is regulated by a voltage applied to a terminal (the gate) insulated from the device. The gate voltage creates an electric field within the device.

2.4.2 CMOS technologies

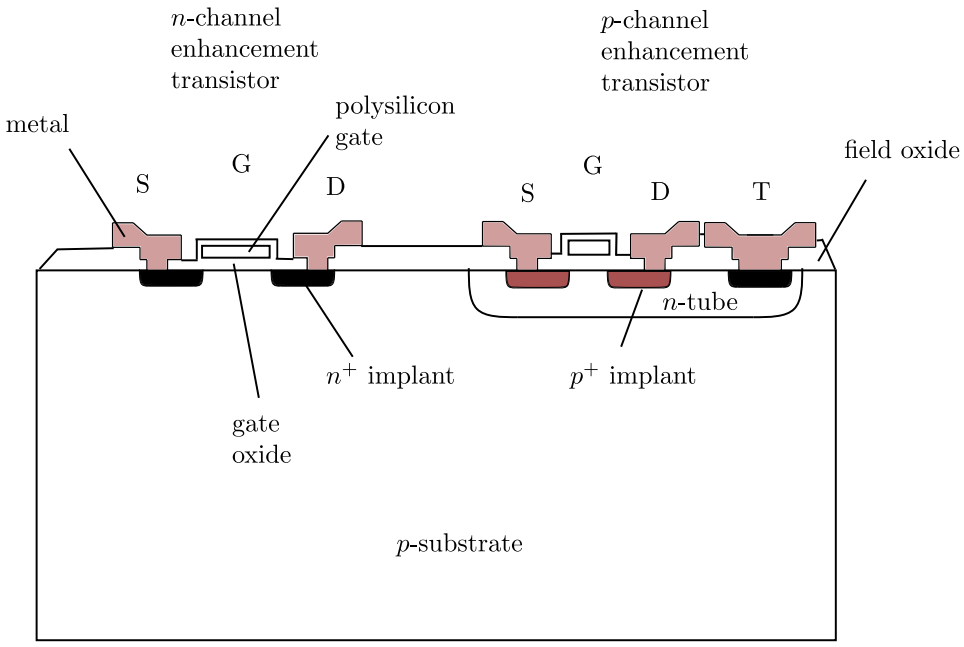


Fig. 2.7: CMOS technology. Cross section through the active devices of a CMOS based on p-type substrate.

CMOS technology is used to implement circuitry on integrated circuits. In its simplest form, it uses only n- and p-channel enhancement transistors as active devices, see Fig. 2.7. The regions between the individual electronic elements are covered by an oxide layer to reduce parasitic capacitances. The source (S) and the drain (D) are heavily n-doped, and the thin gate oxide is covered by a polysilicon gate, which is aligned with the source and the drain. The p-channel transistor is placed in an n-doped well which controls the transistor threshold voltage.

The devices are typically built into a wafer: a common p-type substrate, because p-doped wafers are easier and cheaper to produce. The devices are fabricated on a wafer by layering different materials in specific locations and shapes on top of each other via photolithographic and chemical processes.

The ability to fabricate both nMOS and pMOS on the same substrate made the CMOS technology so successful, e. g. as a radiation sensor, where the sensor and its front-end electronics are both embedded on the same wafer.

ALPIDE sensors (see Chapter 3) use the CMOS Monolithic Active Pixel Sensor (MAPS) technology for all layers.

2.5 Radiation effects

As a natural consequence of using semiconductor pixel sensors for detecting particles in high energy physics, they are exposed to a high flux of ionising particles. That can lead to damage (often irreversible) of both the sensors and electronics.

At the LHC, the typical ranges for detectors to withstand is in the order from kRad[4] up to hundreds of MRad for detectors installed closest to the beam pipe. Comercially made electronics would not withstand that large amounts of radiation, therefore most of the components used in HEP are custom-made.

Radiation induced effects [27], [31] are usually divided into bulk and surface defects. Let us introduce the radiation effects expected to occur in the ALPIDE sensor, the exact values are specified later in Chapter 3.

2.5.1 Bulk damage

Bulk damage are induced by the displacement of lattice atoms due to non-ionising energy loss (NIEL). Using NIEL for scaling allows comparison of damages caused by different types of particles with different energies. Neutrons of 1 MeV are used as reference particles.

- **Leakage current increase**. The leakage current will increase proportionally to the 1 MeV neutron equivalent flux, with proportionality constant being independent of the specific silicon material and the process technology used. The increase then leads to a larger power dissipation of the sensor.

- **Charge trapping**. Macroscopic degradation of the sensor characteristics can lead to trapping of the charge carriers. As a carrier passes the sensor material, the probability of encountering a trap is proportional to the elapsed time. This effect playes an important role in developing the ALPIDE sensors, where diffusion contributes significantly to the charge collection process and collections times may be relatively long.

- **Doping concentration change**. NIEL damage causes an n-type CMOS transistor to become less n-type until the substrate undergoes type inversion to become p-type, as the radiation damage changes the effective dopant concentration by increasing the opposite charges.

[4]Rad is a unit of absorbed radiation dose, defined as 1 rad = 0.01 Gy = 0.01 J/kg.

2.5.2 Surface damage

Ionising radiation is scaled with the total ionising dose (TID), an accumulating effect that becomes worse with time as a device is exposed to ionising radiation. Generating interface states and trapping positive charge carriers in insulation layers, for CMOS transistors, it mainly causes shifts of threshold voltages.

Annealing

To some extent, radiation damage can be repaired by the annealing process. Annealing [32] is a process during which the radiation damage to the detector diminishes over time. Its results are mostly affected by the time of irradiation and temperature used. Each of the mentioned effects has its own specific annealing temperature until which it remains stable - ranging from 90 K up to 600 K.

2.5.3 Single event effects

Besides the bulk and surface damage, single event effects can also occur in the ALPIDE cell, mostly:

- **Single event upset** (SEU). A SEU is associated with the interaction of energetic particles with the substrate close to a sensitive node, causing changes in internal voltages, which can lead to corruption of stored data - a bit flip in a memory cell or register.
- **Single event latch-up** (SEL). A special problem with CMOS electronics is the latch-up [25]. A self-sustaining discharge can be triggered by, for example, electrical pick-up in a $n-p-n-p$ thyristor-type structure built from real and parasitic structures. This leads to a state of drawing abnormally large current.

Chapter 3

ALPIDE silicon sensors

ALPIDE (ALICE pixel detector) is a pixel chip developed by a collaboration formed by CERN, CCNU (Wuhan, China), INFN (Italy), and Yonsei (South Korea). The ALPIDE chip [11], based on the TowerJazz 180 nm CMOS Imaging Process, has been developed by the ALICE pixel groups for both the ITS and MFT upgrade.

The chip contains a novel low-power in-pixel discriminator circuit that drives an in-matrix asynchronous address encoder circuit, read out by an end-of-column lossless data compression and derandomising circuit. The power consumption of the chip is significantly reduced and fast read-out is allowed. The ITS read-out electronics will also be used for the MFT.

Let us outline the main ALPIDE characteristics:

- high-resistivity p-type epitaxial layer (25 μm) on p-type substrate,
- small n-well diode (2 μm diameter) $\implies$ low capacitance ($\sim$fF),
- reverse bias voltage (-6 V$< V_{BB} <$0 V) to substrate to increase depletion zone around n-well collection diode,
- deep p-well shields n-well of pMOS transistors $\longrightarrow$ full CMOS circuitry within active area,
- in-pixel amplification and shaping, discrimination and Multiple-Event Buffers (MEB),
- in-matrix data sparsification,
- on-chip high-speed link (1.2 Gbps),
- low total power consumption ($<$ 40 mW/cm^2).

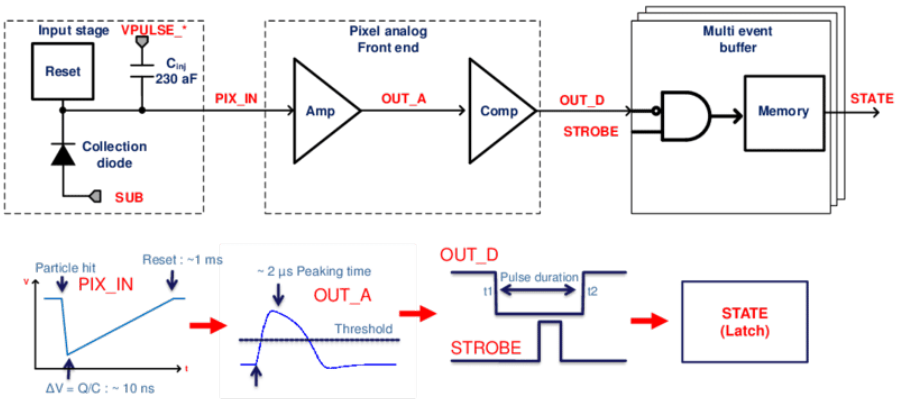


Fig. 3.1: In-pixel hit discrimination block diagram and signal flow. Taken from [33].

3.1 ALPIDE architecture

ALPIDE is implemented on silicon wafers with a high resistivity epitaxial layer. A single chip measures 15 mm × 30 mm and contains half a million pixels distributed in 512 rows and 1024 columns. The block diagram of the ALPIDE pixel cell is shown in Fig. 3.1. A `STROBE` signal controls a threshold level, applied to all the pixels. The ALPIDE architecture also allows to apply reverse substrate bias V_{BB} to increase the total bias of the collection diode.

All the analog signals required by the front-end are generated by a set of on-chip 8-bit digital-to-analog converters (DAC). Analog monitoring pads are available to monitor the output of the DACs.

Communication with the chip uses three paths: slow control, clock and data connections. Slow control and chip-to-chip communication run at a much slower data rate than the high-speed output. The master clock at the LHC runs at 40 MHz and is connected to the chips via a multi-drop line. The same happens for the slow control, which runs with the same frequency.

3.1.1 ALPIDE front-end circuitry

The process of charge amplification and discrimination can be understood from the internal front-end circuit [34] of the ALPIDE cell - Fig. 3.2.

A voltage drop in the `pix_in` node is caused either by the charge collected in the collection diode `D1` or injected through the capacitance C_{inj}. This allows for an additional current flow through the pMOS cascade (`M1, M2`) from the current source `IBIAS`, charging the `pix_out` node. The node is restored as the voltage becomes close to the gate potential `VCASN` of the `M5` transistor and its conductance is reduced. The value of the `VCASN` voltage thus sets the baseline

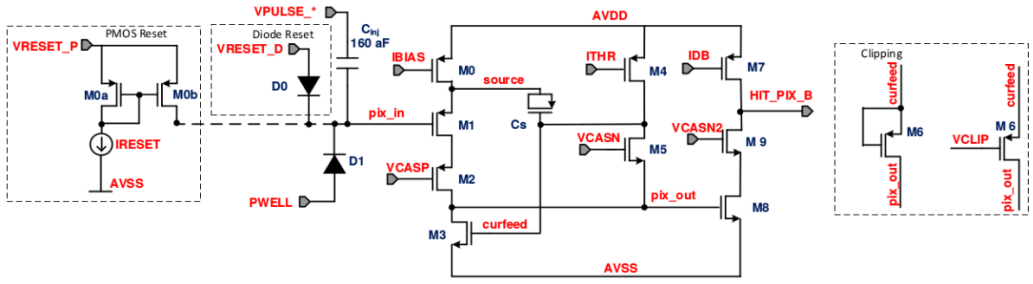


Fig. 3.2: In-pixel front-end circuitry of ALPIDE chip. Taken from [35].

of the `pix_out` potential. The current `ITHR` will therefore flow through the `curfeed` node, opening the `M3` transistor and discharging the `pix_out` node. The duration of the restoration process and the pulse shape can be adjusted with the `ITHR` current. The transistor `M7` becomes conductive again and the `curfeed` node is also restored.

The front-end electronics is completed by a novel read-out approach, faster than the traditional rolling shutter method.

3.1.2 Monolithic Active Pixel Sensor

In the MAPS (Monolithic Active Pixel Sensor) implementation [10], the epitaxial layer is used as a radiation sensitive volume of a detector, with a diode n-well or p-epitaxy layer working as a charge collecting element. With the detector only partially depleted, the charge is collected mainly through a thermal diffusion mechanism. Volume spread of diffusing electrons created by the absorption of radiation is limited by a potential minimum in the middle of the epitaxial layer[1].

A potential barrier is formed between the lightly doped p-type epitaxial layer and the heavily doped p-type substrate that deflects the generated electrons. The signal charge is prevented from diffusing into the substrate by another potential barrier between substrate and epitaxial layer.

The electrons, randomly diffused in the epitaxial layer due to a potential barrier between the lightly doped epitaxial layer and the heavily doped p-wells of the nMOS transistors, are guided towards the n-well of the collection diode.

A typical collection time is in the order of 100 ns. The detector active volume is limited to the epitaxial layer only (with a typical thickness of the order of 10 μm). The total amount of available charge created by minimum ionising particle is a few hundreds of electrons.

[1]The minimum in the middle of the epitaxial layer is created thanks to a particular doping profile.

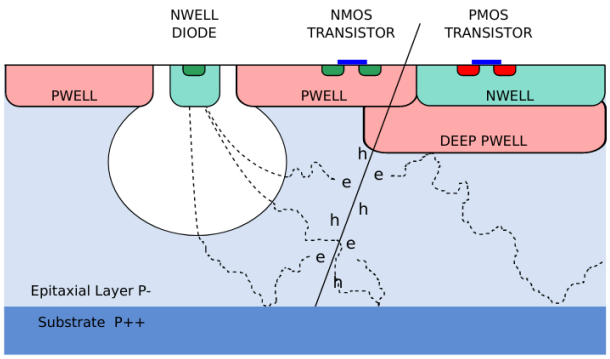


Fig. 3.3: Schematic cross section of a MAPS pixel in the Tower Jazz imaging CMOS with the deep p-well feature. Taken from [11].

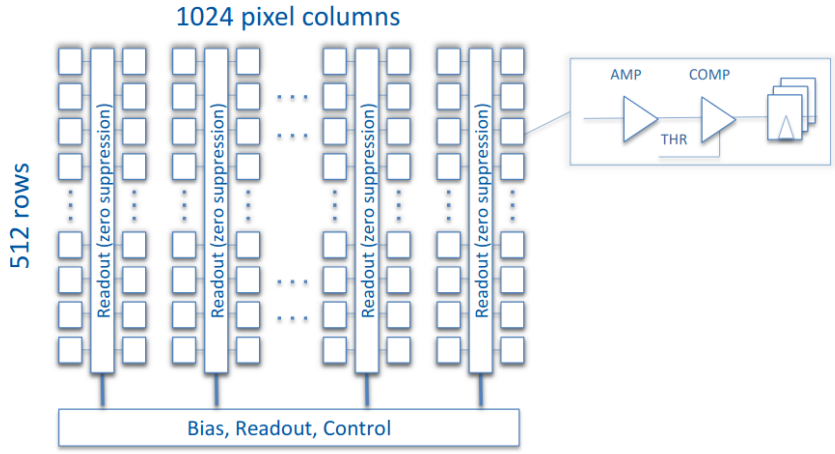


Fig. 3.4: ALPIDE architecture. See text for more details. Taken from [33].

Charged particles generate a thin trail of electron-hole pairs in the silicon (see Fig. 3.3). The entire amount of electrons created due to the passage of ionising particles will be collected, as there is only one p-n junction present in the pixel. The sensor is therefore able to detect particles regardless of where they hit the sensor.

3.1.3 Read-out architecture

An architecture for the read-out of ALPIDE chip is shown in Fig. 3.4. One part of the processes is done in-pixel, namely amplification and discrimination, the pixel also contains 3 hit storage registers. A pitch of 29×27 μm^2 is used, the front-end is continuously active, the chip uses a global shutter and zero-suppressed matrix read-out.

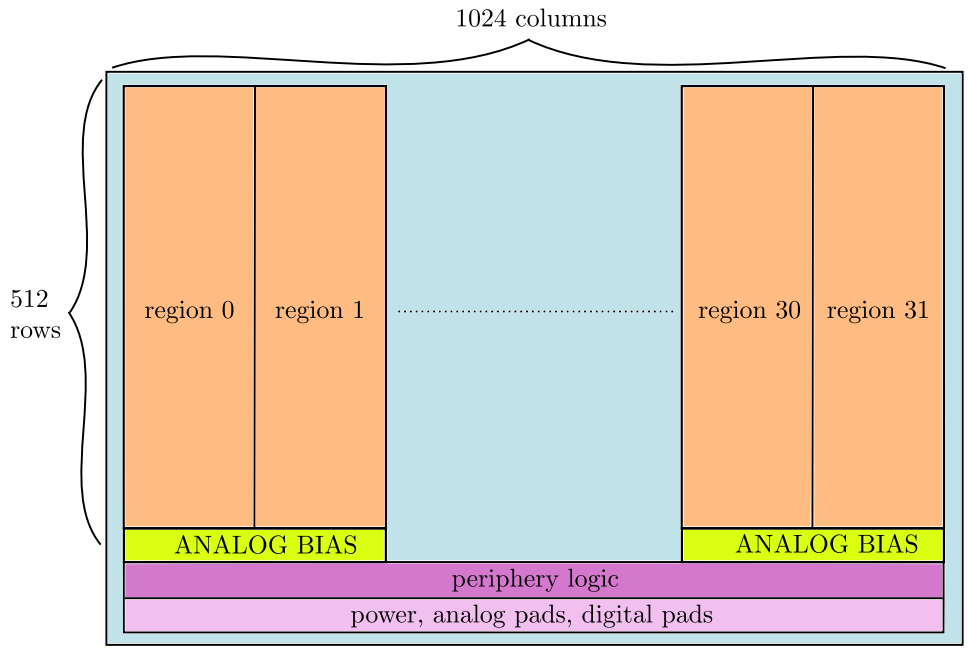


Fig. 3.5: ALPIDE region numbering, see text for details. Taken from [36]

Out of many read-out types proposed [11], the data-driven read-out is used, in which the digital outputs of the pixels are fed into an encoder circuit that generates directly the address of a hit pixel. This can, in turn, be used to reset that particular pixel and go to the next valid one; the procedure is iterated until all pixels are read out. The big advantage, in addition to the low power consumption, is the fast read-out time.

In Fig. 3.5, the chip with digital periphery in the bottom is shown. The 32 regions (512×32 pixels), called region read-out units (RRUS), are numbered $0 - 31$ starting from the left side. The matrix of pixels is read out by an array of 512 priority encoder blocks. The pixels are arranged in double columns and the regions at the middle of each double column are occupied by the priority encoders, which define the indexing of the pixels. During one hit transfer cycle, a pixel with a hit is selected, its address is generated and transmitted to the periphery and, finally, the in-pixel memory is reset. The cycle is repeated until all the addresses of all pixels have been processed and all the pixel state registers have been reset.

3.2 Radiation hardness

Ionising radiation essentially affects the TowerJazz 180 nm technology used in ALPIDE chips. The most noticeable radiation-induced effects are [37]:

- **TID**: after irradiating nMOS and pMOS structures with X-rays up to a dose of 10 MRad, the most affected structures are the 180 nm transistors that show a threshold voltage of a few 10 mV at maximum and an almost complete recovery after 24 hours of annealing,
- **NIEL**: after irradiation with a fluency of up to 1×10^{13} MeVn_{eq}/cm^2, an acceptable decrease of signal-to-noise ratio of 10-20% and an increase of noise of up to 20 % was observed,
- **SEE**:
  - SEU: the test structures were exposed to proton beams between 24 and 230 MeV/c and the bit flips were monitored as a function of exposure time and particle flux and a mean probability lower than 10^{-9} was obtained,
  - SEL: the latch-up has been tested using a memory chip and a full sensor prototype chip. It was found that the sensitivity to latch-up almost entirely resides in the analog block of the ALPIDE prototype.

Characterisation of highly irradiated chips using proton beams was performed at the Nuclear Physics Institute in Řež near Prague, see [38].

3.3 Chip performance and tests

Producing the ALPIDE chip involves numerous difficulties. Relatively high demands need to be met; for example, only one out of 10^5 pixels is allowed to be faulty. As the production of ALPIDE chips takes place in Israel from where the chips are shipped to CERN, there is a possibility of a mechanical damage.

Due to the mentioned facts, to ensure the quality of all the sensors, prior to mounting on the stave or the ladder, each chip is tested according to a defined test procedure. All the tests are performed with and without back-bias. A basic electrical test (also called *smoke test*) is performed first. The electrical and functional tests address the full electrical functionality of the chip and validate the signal generation in the epitaxial layer.

Sensor response is studied using either light or a radioactive source.

During chip testing, a probe card is used to provide the electrical connection to the chip pads. Functional tests include the read-out test, FIFO (first in - first out) scan, digital scan, threshold scan, noise occupancy scan, and eye measurement.

Later on, the same qualification process has been performed for chips assembled in a ladder. Ladder qualification was the crux of my work at CERN, therefore all the tests will be further described in Chapter 5.

Chapter 4

The Muon Forward Tracker

The MFT was proposed to be added to the current detector system in ALICE as a part of upgrade during the Long Shutdown 2. Hard processes in a collision are sensitive probes providing us with a detailed description of the deconfined medium. The upgrade program was thus aimed to reach a high precision measurement of these probes with an upgrade of the ITS and the MFT. The physics motivation for the MFT will be further dicussed in my master's thesis; in the first section of this chapter, we only briefly report the main goals. This chapter also contains a brief description of the MFT layout.

4.1 Physics motivation for the MFT

The presence of the MFT will enhance ALICE capabilities for detecting muons at forward rapidity [39]. Mainly, it will generally improve all the measurements performed by the Muon Spectrometer. On top of that, new physics will become accessible down to very low p_T: separation of prompt and displaced J/ψ or separation of charm and beauty decays. ALICE with the MFT will provide an excellent tool to perform such measurements [39].

Amongst the many other physics objectives of the upgraded ALICE detector [20], we will focus in the following paragraphs on the motivation for the study of open heavy flavours, charmonia and low-mass dimuons.

4.1.1 Current physics limitations

With the Muon Spectrometer alone, the measurements suffer from several limitations, mainly due to the multiple scattering induced on the muon track by the hadron absorber [39]. From the spectrometer, the tracks do not constraint in the region of the primary vertex. Information about the details of the vertex region is lost, which makes it impossible to distinguish the background represented by muons coming from semi-muonic decays of π and K mesons, often

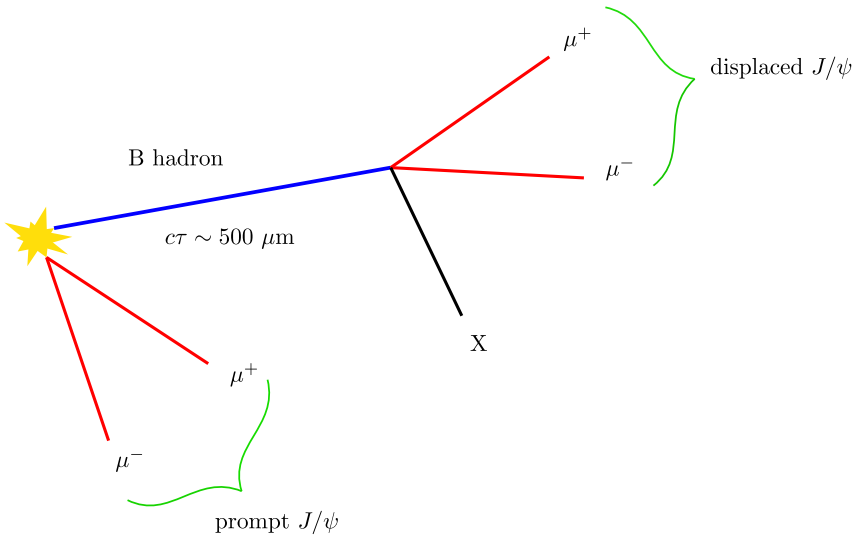


Fig. 4.1: Diagram of prompt and displaced J/ψ decaying into dimuons.

used in muon analyses. Limited details in the vertex region also prevent us from disentagling of open charm and open beauty production or distinguishing between prompt and displaced J/ψ production (see Fig. 4.1).

4.1.2 Open heavy flavours and quarkonia

Heavy flavour production serves as an important probe of the medium produced in ultra-relativistic heavy-ion collisions. Charm and beauty quarks with their large masses ($m_c = 1.27$ GeV, $m_b = 4.18$ GeV, [40]) play an important role in probing the early stages of the collision. On the other hand, charm and beauty hadrons have a long lifetime ($c\tau \sim 150$ μm and $c\tau \sim 500$ μm [41]), which provides us with information about the evolution of the deconfined medium.

The nuclear modification factor

$$R_{AA}(p_T) = \frac{1}{\langle N_{coll} \rangle} \cdot \frac{dN_{AA}/dp_T}{dN_{pp}/dp_T}, \tag{4.1}$$

is used to study the evolution of the medium considering the energy loss of heavy quarks. Here, $\langle N_{coll} \rangle$ is the mean number of binary collisions[1], $dN_{AA}/dp_T, dN_{pp}/dp_T$ are the production yields as a function of transverse momentum in nucleus-nucleus (AA) and pp collisions.

According to QCD, quarks should lose less energy than gluons when passing through the medium. This is due to the fact that in-medium gluon radiation is expected to increase with the colour-charge of the emitting particle. The

[1] N_{coll} can be analytically derived from the Glauber model [42].

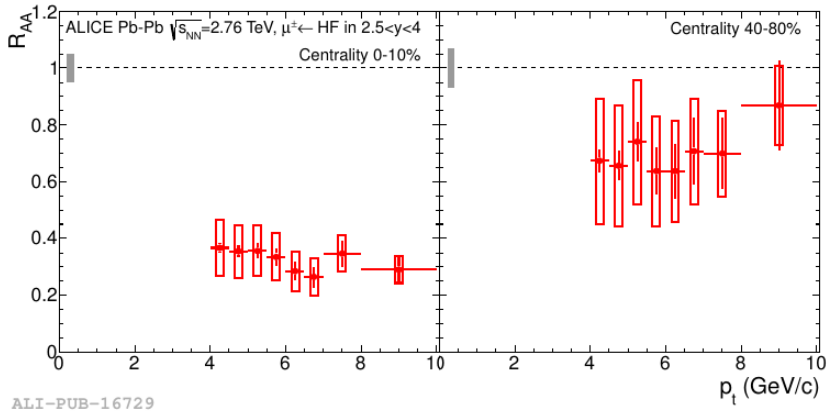


Fig. 4.2: R_{AA} of muons from heavy-flavour decays in $2.5 < y < 4$ as a function of p_T in different centrality classes in Pb–Pb collisions at $\sqrt{s_{NN}} = 2.76$ TeV. Open boxes represent the systematic uncertainty. Taken from [39].

energy loss should further decrease with increasing mass, due to the so-called *dead-cone* effect, where gluon radiation is suppressed below certain radiation angle. Having a larger minimal angle below which no radiation occurs, heavy quarks radiate less gluons, which results in the observation of a smaller energy loss. Due to their colour charge, gluons, dominating the production of light hadrons, are expected to lose more energy than quarks but also, charm quarks are expected to lose more energy than beauty quarks due to their smaller mass. For the nuclear modification factors, all of the mentioned should result in

$$R^{\pi}_{\mathrm{AA}} < R^{D}_{\mathrm{AA}} < R^{B}_{\mathrm{AA}}. \tag{4.2}$$

The present status of heavy-flavour measurements in heavy-ion collisions at forward rapidity is shown in 4.2. The present measurement in the forward-rapidity region suffers from being inclusive and from being limited to high p_T.

The MFT will allow us to measure the production cross section of muons from charm and beauty decays separately down to low p_T. The effect of a separate measurement provides a reference for the study of charmonium/bottomonium suppression in the QGP and measuring the charm and beauty R_{AA} separately allows us to test theoretical predictions for the energy loss of charm and beauty quarks in the medium.

4.1.3 Charmonia

Considering charmonia production, measurements are currently limited by a large combinatorial background and the impossibility to disentangle prompt and displaced production.

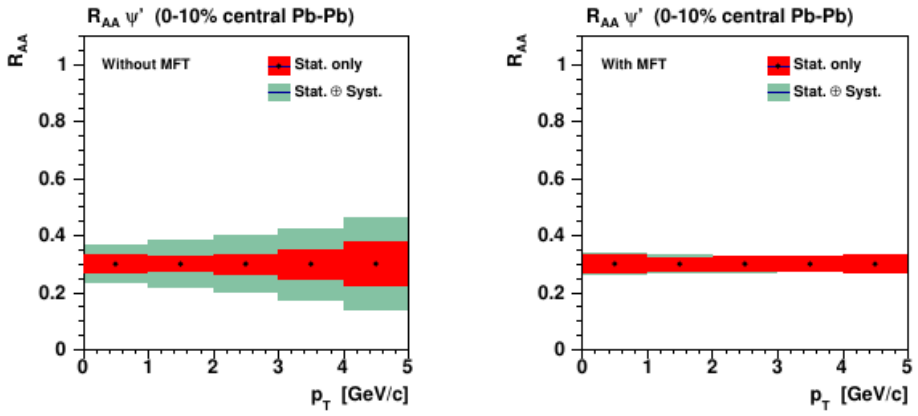


Fig. 4.3: Expected uncertainties on the measurement of R_{AA} of the ψ', in the scenario without and with MFT, where $R_{AA}(\psi') = 0.3$ is considered. Taken from [45].

Charmonia production is the classical tool to investigate:

- suppression mechanisms due to dissociation of charmonia states in the medium (colour screening) [43],
- recombination mechanisms due to the relative abundance of available $c\bar{c}$ pairs in the deconfined medium [44],
- the interplay between suppression and recombination mechanisms.

The presence of the MFT detector will significantly reduce the uncertainties on the extraction of the ψ' signal by improving the signal over background (S/B) ratio and allow for a reliable separation of prompt and displaced J/ψ production. Currently, with the Muon Spectormeter alone, the S/B ratio ranges from 0.2% to 0.5% according to the p_T range [45]. Thanks to the capability of the MFT to access the details in the vertex region, both muon pairs where at least one muon is produced within the hadron absorber, and muon pairs whose muons do not share a common origin, could be identified and rejected.

The MFT will therefore improve the ψ' measurement in the most central collisions and will allow for the first time for the measurement of the ψ' R_{AA} as a function of p_T.

4.1.4 Low-mass dimuons

Low mass vector meson (ρ, ω, φ) production provides key information on the hot and dense state of the the strongly interacting matter which is produced in

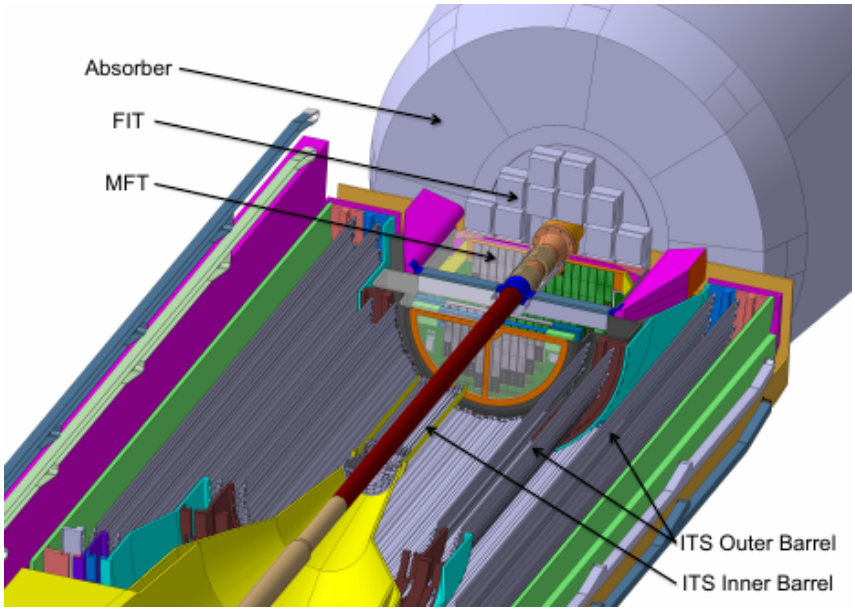


Fig. 4.4: Positioning of the MFT detector in ALICE. Taken from [37].

high-energy heavy-ion collisions. Insights on non-perturbative QCD are also provided [41].

Dileptons are an important probe of the temperature and the dynamical properties of the QGP. As they are emmited at every stage of the matter evolution, the observed dilepton spectra contains information about the entire history of the evolution.

The necessity to subtract the large combinatorial background coming from semi-muonic decays of pions and kaons in order to properly identify low-mass dimuon spectra represents a challenging task. The MFT will significantly improve the performance of ALICE for the measurement of dimuons at forward rapidities.

4.2 MFT Layout

The design of the MFT was constrained by requirements expressed by ALICE and the LHC [20]. The importance and the layout of the detector was stated in the Addendum to the ALICE upgrade Letter of Intent [39], the design itself was further presented in the MFT Technical Design Report [37].

The MFT is holding the beam pipe and is surrounded by other detectors, to which the MFT should not introduce any mechanical or thermal perturbations. The design also allows maintenance without moving the TPC in as short time as possible to be done during the LHC winter shutdowns.

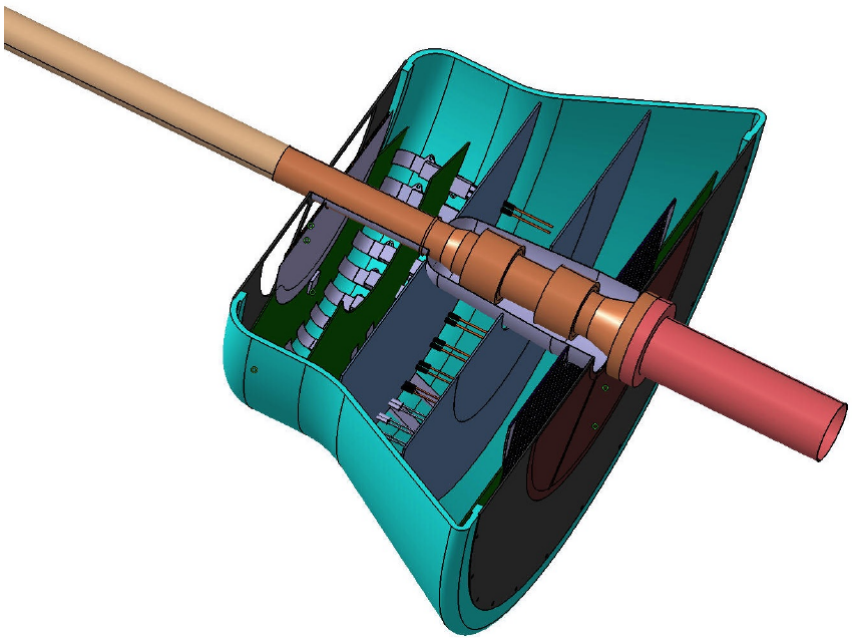


Fig. 4.5: Layout of one half of the MFT detector. Taken from [39].

The MFT has a conical shape surrounding the beam pipe and is placed between the IP and the hadron absorber. A general view of the MFT is shown in Fig. 4.4 and 4.5. The detector consists of two half-cones. Each MFT half-cone consists of 5 half-disks positioned along the beam axis in the direction of the Muon Spectrometer at $z = -460, -493, -531, -687, -768$ mm from the IP. The MFT covers the pseudorapidity acceptance $-3.6 < \eta < -2.45$.

A half-disk consists mainly of sensor ladders, containing 2 to 5 silicon pixel sensors soldered to a flexible printed circuit (FPC).

Special care has been taken in selecting materials to minimise the material budget[2]; it amounts to less then 0.6% of a radiation length X_0 per disk.

4.2.1 Pixel sensor

The basic detection element of the MFT is a silicon pixel sensor ALPIDE that was further described in Chapter 3.

4.2.2 Ladder structure

The silicon pixel sensors are integrated on mechanical ladder structures that hold the sensors and ensure electrical links between the sensors and the read-

[2]The radiation length X_0 is commonly used to determine the amount of material traversed by particles in a detector. The detector thickness expressed in units of X_0 is called the *material budget*.

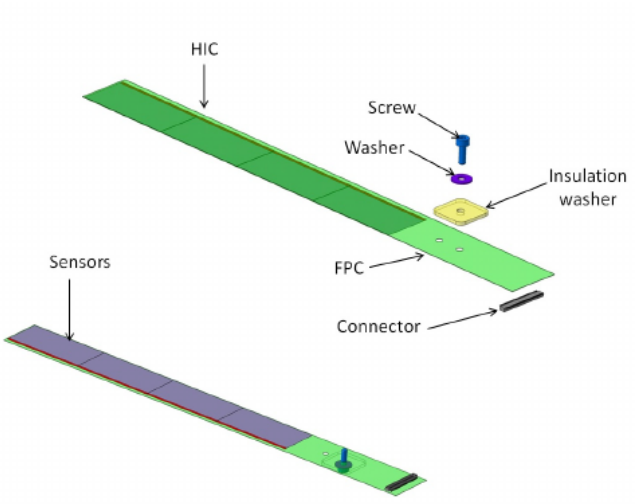


Fig. 4.6: Details of the MFT ladder in top exploded view and bottom view. Taken from [37].

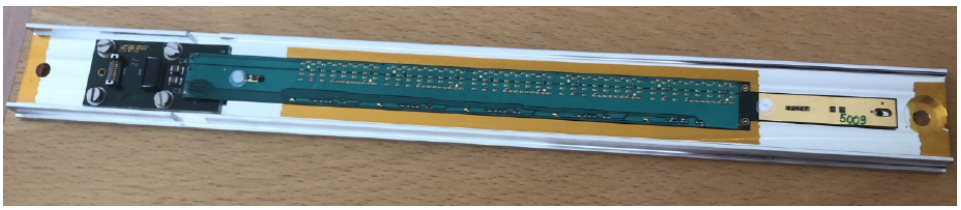


Fig. 4.7: Ladder after the assembly, prepared for the qualification tests.

out electronics. A ladder consists of the following elements (Fig. 4.6): the stiffener, serving as a mechanical support, the silicon pixel sensors and the FPC. An actual photo of ladder in a protective cover is in Fig. 4.7.

The Hybrid Integrated Circuit (HIC) consists of the sensors laser-soldered to the FPC with a gap of 100 μm between sensors.

The ladder assembly and qualification procedure are further described in Chapters 3 and 5.

4.2.3 Disk and global support structures

The MFT consists of five disks. The first two of the disks (called Disk-0 and 1) located closer to the IP are identical, while the remaining three disks are different and larger (Disk-2, 3 and 4). Each disk is subdivided into two half-disks (4.8). Each half-disk has two detection planes, one on the front and one on the back side. The hermeticity of each half-disk is ensured by the overlap between sensors of the back and front planes.

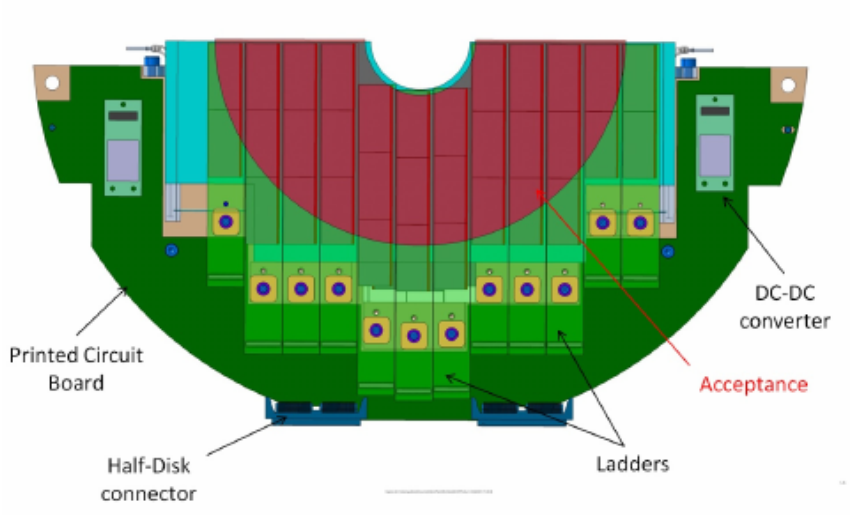


Fig. 4.8: Schematic figure of Half-Disk-0. Taken from [37].

A half-disk consists of a disk spacer, a disk support, two Printed Circuit Boards (PCBs) and the sensor ladders. The PCBs are equipped with connectors, DC-DC converters providing 1.8 V for the sensors and other electronic components. The ladders are fixed on one edge with one screw for safety and glued all along their length on the half-disk spacer.

4.2.4 Read-out architecture and electronics

The read-out architecture system of the MFT is compatible with the CMOS pixel sensor architecture for the data throughput on one side and with the ALICE Common Readout Unit (CRU) on the other side. The constraint for the read-out architecture is the radiation environment of 50 krad at the outer radius of the MFT acceptance, which demands the use of active electronic components in a safer area, where the TID is below few krad. Another constraint is the tight space available for MFT services.

Fig. 4.9 illustrates the MFT read-out scheme for a 100 kHz Pb–Pb minimum bias collision rate. The disk PCBs ensure the transmission of upstream (slow control) and downstream (data) signals as well as the power supply distribution up to the sensors.

The MFT is powered through aluminium bus bars. The upstream and downstream signal are transmitted by twinaxial cables from the MFT cone to an external backend concentrator board, equipped with active components for data concentration. From the backend read-out unit board, data are transferred to the CRU via radiation-hard optical components.

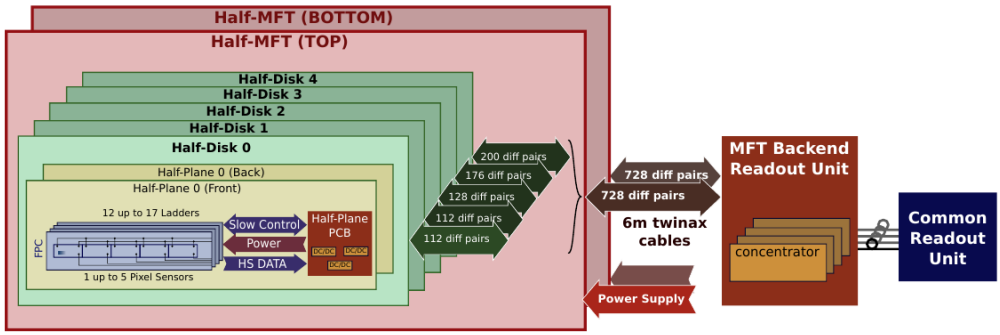


Fig. 4.9: General MFT read-out scheme. Taken from [37].

Chapter 5

Commissioning

With the LHC schedule available at the beginning of this work, the LS2 was foreseen to take place until 2020. The installation of the MFT was foreseen sequentially with the ITS, whilst the commissioning in parallel, over a period of three months near the end of the LS2. In the meanwhile, the LS2 schedule has suffered modifications and is still not completely fixed.

The following sections describe the work on the ladder assembly and qualification procedures that I participated in at CERN, including the description of the main steps of the procedures. The fundamental principles for understanding the behaviour of the ladders are presented, as well as the requirements for different result of ladders qualification.

5.1 Hybrid Integrated Circuit and Ladder Assembly

Prior to mounting on the ladder, each chip was tested via an automatic procedure using a probe card equipped with micrometric needles. The needles are put in contact with the pads of the ALPIDE chip in order to interconnect the chip to the card and run a series of qualification tests, such as power consumption test, memory access, DAC calibration or threshold scans. The results of the tests are stored in a database common for the MFT and the ITS.

The FPC needs to be prepared (using a procedure called *shaving*) and cleaned, using an ultrasonic bath. Any defects, that is cracks, exceeding solder paste, and foreign substances on the FPC are reported.

The main requirements for the ladder assembly are a reliable high quality technique to connect the pixel chips to the FPC and a placement accuracy of each chip in the order of μm. The interconnection between the FPC and the chips is ensured by micro-wire ultrasonic bonding.

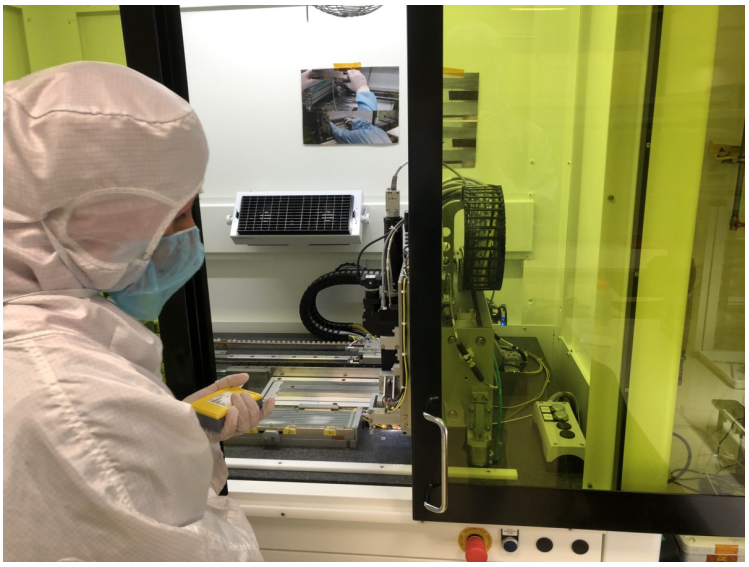


Fig. 5.1: ALICIA machine for ladder assembly. The machine is located in a cleanroom at Department Silicon Facility (DSF) at CERN.

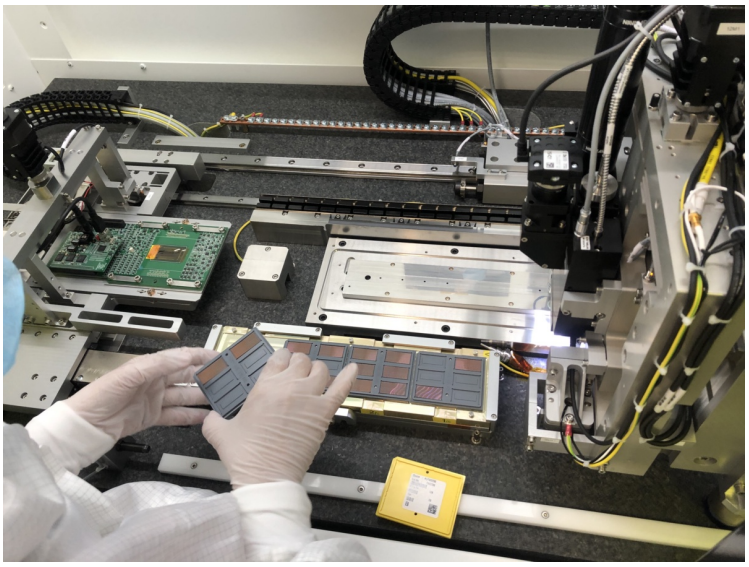


Fig. 5.2: Chips positioning in the ALICIA machine. After being picked from the wafer, chips are stored in trays. A combination of chips satisfying the desired qualification result is chosen for ladder assembly.

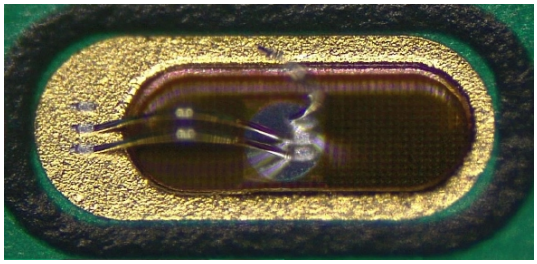


Fig. 5.3: 25 μm wire bonds used in the HIC. In the photo, one of the wire bonds has failed the pull test.

A system called ALICIA (*ALICE Integrated Circuit Inspection and Assembly machine*), often called MAM (Module Assembly Machine) (see Fig. 5.1 and 5.2) is used for an automated inspection and assembly of chips on an FPC. The chip quality (dimensions inspection, edge integrity, pad cleanliness) is inspected by the high resolution vision system. In order to give ALICE the required accuracy, ALICIA uses a high-accuracy (< 0.1 μm) image system. In a final assembly, the accuracy of < 5 μm over the full array of chips is achieved.

After the chips were inspected and positioned using a vacuum gripper, they are glued to the FPC. The glue polymerisation takes 4 hours. Thereafter, the HIC is placed in the wire bonding machine. Wire bonds are interconnections between the FPC and chips made with a 25 μm wire. Three wire bonds per pad are created, see Fig. 5.3. Once bonded, a HIC becomes a ladder.

The pull tests of the wire bonds, where the pull strength at which the wire bond fails is determined, are performed to test the mechanical properties. Wire bonds need to be protected during further manipulation with the ladder.

Performing the described steps makes the ladder prepared for the qualification tests.

5.2 Ladder quality assurance

Ladder qualification is a crucial tool in the process of building the MFT detector.

A visual inspection is carried out to reveal any mechanical damage that could have been inflicted during the assembly.

The qualification process consists of several stages: electrical tests, following a similar, though more light-weight procedure as the single chip tests, functional tests, and the eye measurement.

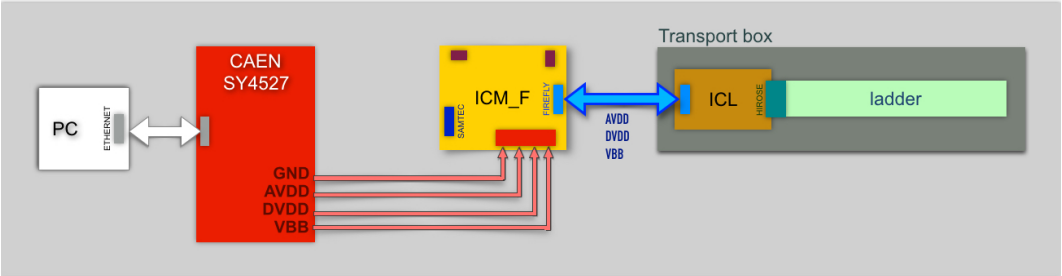


Fig. 5.4: Test bench used for the smoke test.

5.2.1 Smoke test

The term *smoke test* refers to a test when the ladder, or generally a circuit, is attached to power for the first time, which could, in some cases, actually produce smoke—which would mean the circuit is faulty and there is no need to do more testing.

To perform the smoke test and following tests, the ladder is connected to an ICL card (*Intermediate Card for Ladder*), which provides an electric interface between the ladder and the test-bench read-out, see Fig. 5.4.

A maximum voltage `AVDD` and `DVDD` is set to 1.8 V and for back bias voltage $V_{\mathrm{BB}} = -3$ V. In the smoke test, the power is ramped-up gradually via a remotely controlled system. This is very useful to spot short circuits and also tansient overcurrent that stabilise and allow further operation. Any eventual abnormalities in current can be visually noticed in the GUI shown in Fig. 5.5, which results in aborting all the tests and there is an extra intervention required to fix the eventual problems.

5.2.2 Electrical tests

Electrical tests consist of three parts. In the first part, called `test A`, the power is sent to the ladder and the total power consumption of the ladder is tested. With both `AVDD` and `DVDD` fixed at 1.8 V, the current consumption is noted. In the `test B`, the clock signal is also sent to ladder. Finally, `test C` applies power, clock as well as activity on all chips. The `test C` therefore represents a simultaneous digital scan on all working chips.

5.2.3 Ladder functional tests

The power supply used for the functional tests provides a voltage of 5 V. However, the operating voltage of the ALPIDE chip is only 1.8 V, so there is a power converter used for the transition between these two voltages.

Fig. 5.5: Results of the smoke test as shown on the GUI.

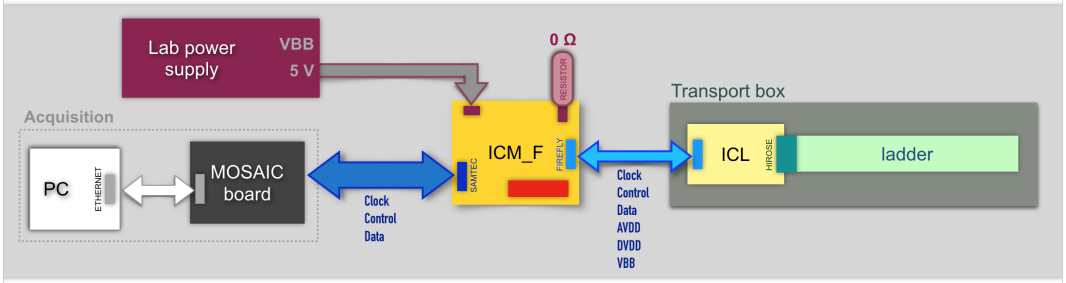


Fig. 5.6: Test bench hardware for functional tests without back bias: $V_{\mathrm{BB}} = 0$ V.

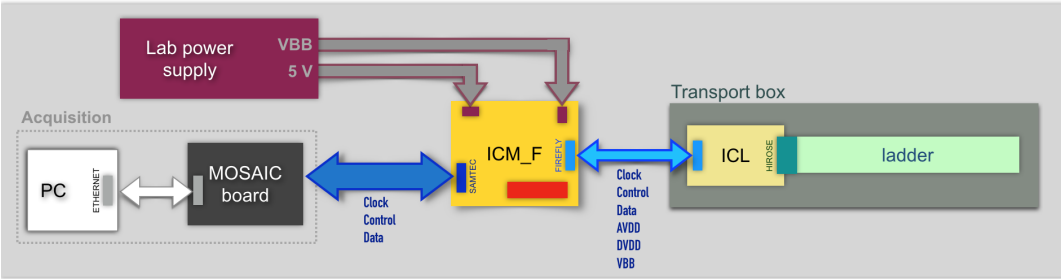


Fig. 5.7: Test bench hardware for functional tests with back bias $V_{\mathrm{BB}} - 3$ V.

All the functional tests are done with the test benches without back bias voltage ($V_{\mathrm{BB}} = 0$ V) and with back bias ($V_{\mathrm{BB}} = -3$ V), where the 0 Ω resistor terminator in the `ICM_F` board is replaced by a negative potential supplied by the laboratory power supply, see Fig. 5.6 and 5.7. The `ICM` (Intermediate Card for MOSAIC) represents an adaptation board providing power regulation and data connector adaptation to the MOSAIC data acquisition system.

A 5 V voltage is delivered for the analog and digital voltages from the laboratory power supply. An ICL card is used to provide the power for the ladder and also to send the data to the MOSAIC board [46], which is used for testing configuration and read-out, that conducts the measurements on the chip commanded by the computer. ALPIDE testing software [47] is used to control the tests via the GUI window and to gather the results.

Read-out test

The read-out test checks the reading/writing configuration (I/O connection) and writing to chips' registers—the clock is active and provided to all the chips. The read-out test, executed by the software prior to all other functional tests, verifies only the slow control circuitry of the chip—the digital and analog parts are not tested here.

If any chip in the ladder is found to be not responding, there is an option to disable it and proceed with the functional tests for all the other enabled chips.

FIFO scan

An ALPIDE chip contains around 100 registers — small blocks of memory with one particular task, mostly, they are used to save variables and data. A FIFO (*first in, first out*) test is a simple test checking the registers if they are storing the data in the right way - the first (oldest) entry is processed first.

A sequence of bits is sent to the the register if it is available for the write and read actions. After a while, the read-out of the register is performed to see if the sequence differs from or corresponds to the initial one.

There are two possible results of the test: GOLD and RED, where two or more errors in the FIFO test result in RED. All the ladders with the RED results are considered non-conformal.

Digital scan

A digital scan tests the behaviour of the digital part of the chip (e.g. using a test pulse pattern). Using a test pulse pattern, each pixel is pulsed 50 times. In this manner, dead, inefficient and noisy pixels are detected:

- if a pixel does not respond at all, it is considered **dead**,
- if a pixel responds at least one time but less than 50, it is considered **inefficient**,
- if a pixel responds *more* than 50 times, it is considered **noisy**.

Therefore, only the pixels from which we get exactly 50 responses are considered conformal. If we label the dead, inefficient and noisy pixels as *faulty* pixels, the outcome of the digital scan results from the number of faulty pixels n_f:

- $0 \leq n_f < 50 \Rightarrow$ GOLD
- $50 \leq n_f < 2100 \Rightarrow$ SILVER
- $2100 \leq n_f < 5243 \Rightarrow$ BRONZE
- $n_f \geq 5243 \Rightarrow$ RED.

Ladders with GOLD, SILVER and BRONZE result of the digital scan are marked conformal.

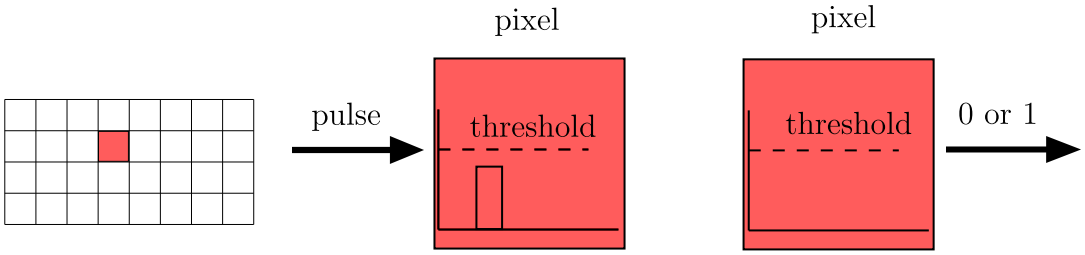


Fig. 5.8: An overview of the steps performed by a threshold test: a pixel is selected, while the rest of the chip is masked. A pulse is injected into the pixel and finally, the value in pixel's memory is read.

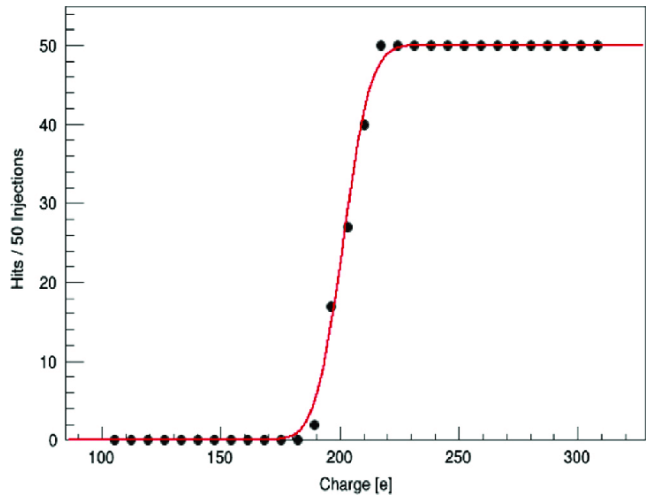


Fig. 5.9: A threshold S-curve for the front-end pixel chip. The input level of electrons of the injected pulse is plotted against the number of hits detected in the pixel out of 50 measurements - the threshold can be seen as the number of electrons where the number of hits reaches 50%. Taken from [48].

Threshold scan

The stages of the threshold scan are illustrated in Fig. 5.8. After a specific pixel was selected and the rest were masked, an analog pulse resembling a particle hit is injected into the pixel. The height of the pulse is an analogue to the energy of the particle.

The value of injected charge at which the pixel starts to detect particles is extracted as a result of the threshold scan. An increasing charge q_{inj} is injected $N_{\text{inj}} = 50$ times through the injection capacitance C_{inj}. The results are fitted with the following function

$$f\left(q_{\text{inj}}\right) = \frac{1}{2} N_{\text{inj}} \left[1 + \text{erf}\left(\frac{q_{\text{inj}} - q_{\text{thr}}}{\sqrt{2\sigma}}\right)\right], \tag{5.1}$$

where q_{thr} is treated as the threshold - the charge at which a selected pixel registers a hit with a probability of 50%, σ is a parameter—noise, which describes the slope of the increasing function[1], see Fig. 5.9. The noise is defined as the difference in DAC levels where the probability is 10% and 90%.

The threshold value varies from pixel to another. The test therefore needs to be performed for multiple pixels. After the threshold is obtained for each pixel in the selection, a histogram is created - thus a distribution of threshold and noise for each chip in the ladder is created, see Fig. 5.10.

Generally, the threshold and noise mainly depend on `ITHR` and `VCASN` values. The value of threshold is approximately linearly increasing proportionally to the `ITHR` value. For the `VCASN` value, the situation is the opposite: the threshold decreases with increasing `VCASN`. In the tuned threshold scan, both parameters are set such that all the pixels in the matrix have a uniform threshold value [34].

Similarly to the digital scan - ladders are ranked according to the number of faulty pixels. If the threshold is unrealistically high, we can detect a *dead* pixel. In the same way, if the threshold of a pixel is 0, we can assume a *stuck* pixel. Ladders with the RED result of the threshold scan are treated as non-conformal.

Noise occupancy scan

Noise occupancy scan is performed to obtain a fake hit rate, which describes the probability of registering a hit by a pixel when there was no ionising particle passing through the pixel. The noise occupancy is defined as the number of pixels producing a fake hit divided by the total number of pixels in the chip. The ALICE upgrade plans [20] require a noise occupancy below 10^{-5}hits/event/pixel, corresponding to about 5 fake hits per event per chip.

[1] Noise in fact represents the standard deviation of the derivative of $f\left(q_{\text{inj}}\right)$.

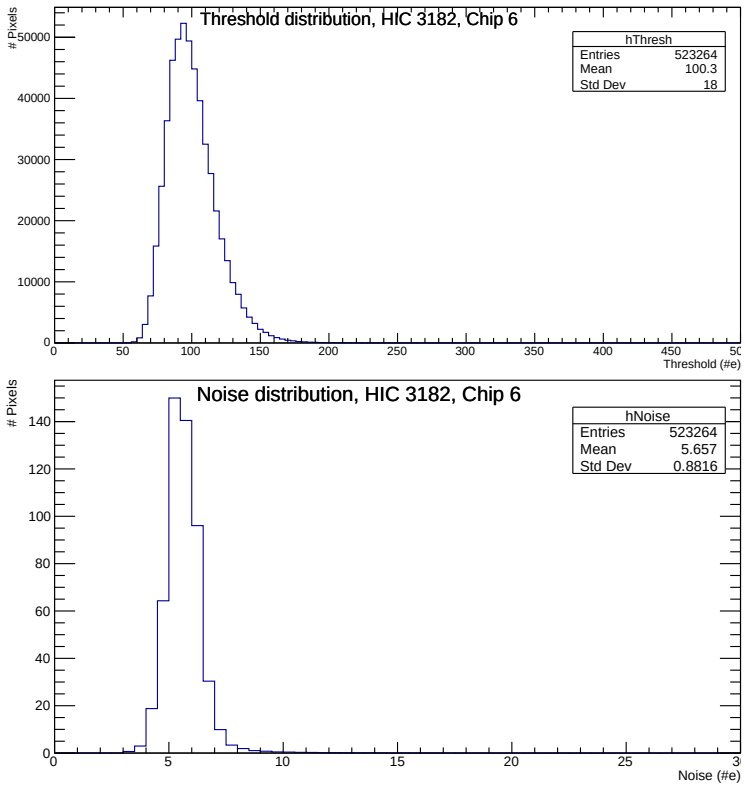


Fig. 5.10: Result of the threshold scan for chip 6 in ladder HIC_3182.

In the noise occupancy test, a large number of random triggers from the MOSAIC board is produced and the number of registered hits is then read by the board. Most of the noise is produced by the so-called *hot* pixels: pixels with an increased probability of producing a hit in comparison to the rest of the pixels. Masking a small amount of pixels [35] can significantly reduce the fake hit rate.

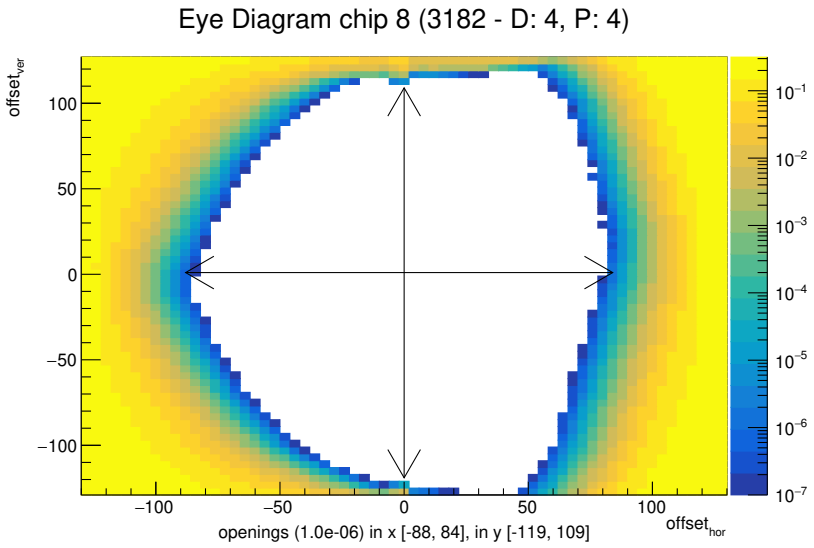


Fig. 5.11: Measured eye diagram for chip 8 in ladder HIC_3182.

Eye measurement

Measuring the eye diagram is a general-purpose tool for analysing digital signals. It is a synchronised superposition of all possible realisations of the signal of interest viewed within a particular signaling interval.

Starting from a digital waveform, the parts of the waveform corresponding to each individual bit are folded into a single graph. This results in a plot with signal amplitude on the vertical axis and time on the horizontal axis. After repeating the construction with multiple samples of the waveform, the resulting plot represents the average statistics of the signal shape and resembles an eye, see Fig. 5.11.

The eye diagram allows verifying the high speed (1.2 Gbit/s) data transmission capability of the ladder. This is obtained by setting the chip in a particular mode (PRBS mode), in which the MOSAIC and the chip communicate by exchanging fixed pattern data words at the highest speed. The proper transmission of each bit of the words is characterised by the signal transition in time and amplitude from 0 to 1, which is represented by the two axes of the eye diagram.

The eye diagram qualification system is different compared to other tests. Two parameters, horizontal and vertical, are evaluated - namely `X opening` and `Y opening`, the first could be converted to time and the latter to voltage. Possible ranges are reported in [34], ladders with RED result of the eye measurement are considered non-conformal.

The whole qualification is first performed with $V_{\mathrm{BB}} = 0$ V and then repeated at $V_{\mathrm{BB}} = -3$ V.

5.3 Disk and Cone Assembly

The disk supports made from plastic and the heat exchangers with all their components have been designed in SUBATECH in Nantes, France. The heat exchanger is made of a sandwich of two carbon composite cold plates embedded polyimide pipes with 1 mm in diameter and a rigid foam in between. There are multiple tests [34] done at SUBATECH to qualify the heat exchanger.

To supply the power for chips, to transfer data and to allow communication with the ladders, PCBs designed and produced at CCNU, China are used.

After the qualification process, ladders—in case they have been declared conformal—are sent to IPNL in Lyon to be glued on the disk.

The half-MFT cones are assembled at CERN.

The half-MFT assembly proceeds in two steps, first the assembly inside the MFT cone, then the assembly of the MFT cone inside the barrel. Each step

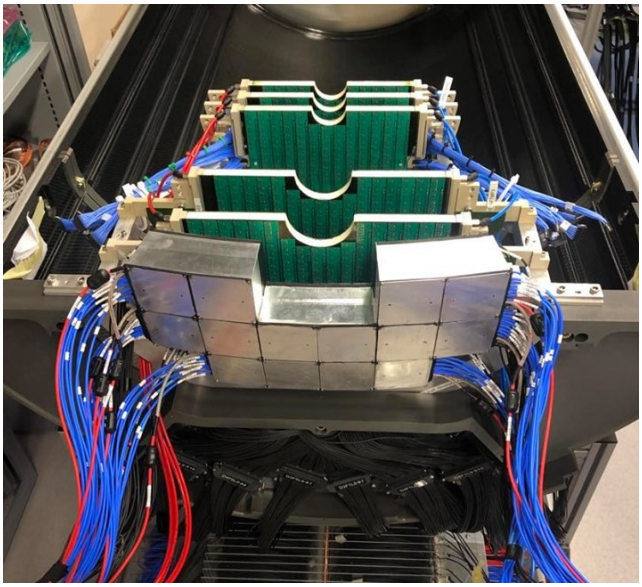


Fig. 5.12: The MFT half-cone assembled inside the barrel. The picture also show cables, cooling tubes and a part of the Fast Ineraction Trigger (T0C+).

starts with servicing with cables for both signals and power, pipes for cooling, which is followed by a pressure test to detect any leakage.

A patch panel is located at the back-end of the cone. To be able to route all the cables from each half-disk to a patch panel, the cone assembly starts with the disk closest to the IP. For each half-disk installed in the cone, an electrical and leak test is performed. Once all five half-disks are installed, a qualification test is performed for about one week. This puts the survey of the disks to an end.

To assemble the MFT cone with the barrel (see Fig. 5.12), the MFT half-cone needs to get mechanically fixed inside the barrel, which is followed by the connection of the cables and cooling tubes to the MFT read-out board and a qualification test of the global assembly is performed for at least 3 months.

The commissioning in ALICE cavern follows.

Chapter 6

Ladder qualification analysis

This chapter summarises the analysis of the ladder qualification programme of all the produced ladders for the MFT. Data from the ladder production database accessible online were used. Results of the tests that are used are stored in a common workspace in `*.xml` files, which had been filled by the tester performing the qualification tests.

Yield of conformal ladders

This analysis is based on the data from the 528 ladders that have been assembled and qualified afterwards. All the plots below consider only conformal ladders, criteria to mark a ladder as conformal ensuing the qualification tests were stated in Chapter 5. The total number of conformal ladders is summarised in Table 1.1 and Figure 6.1. We can see that majority of the produced ladders has been declared conformal, which is, given the complexity of the assembly process, a satisfactory result. There are various reasons why a ladder could have been declared not conformal, e.g. a large number of dead pixels or communication problems resulting in a problematic eye diagram.

LADDERS	2-chip	3-chip	4-chip	5-chip
total amount	57	236	158	21
conformal amount	45	176	134	18
conformal yield	79%	75%	85%	86%

Table 6.1: Summary of the amount of produced and bonded ladders and yield of the conformal ones.

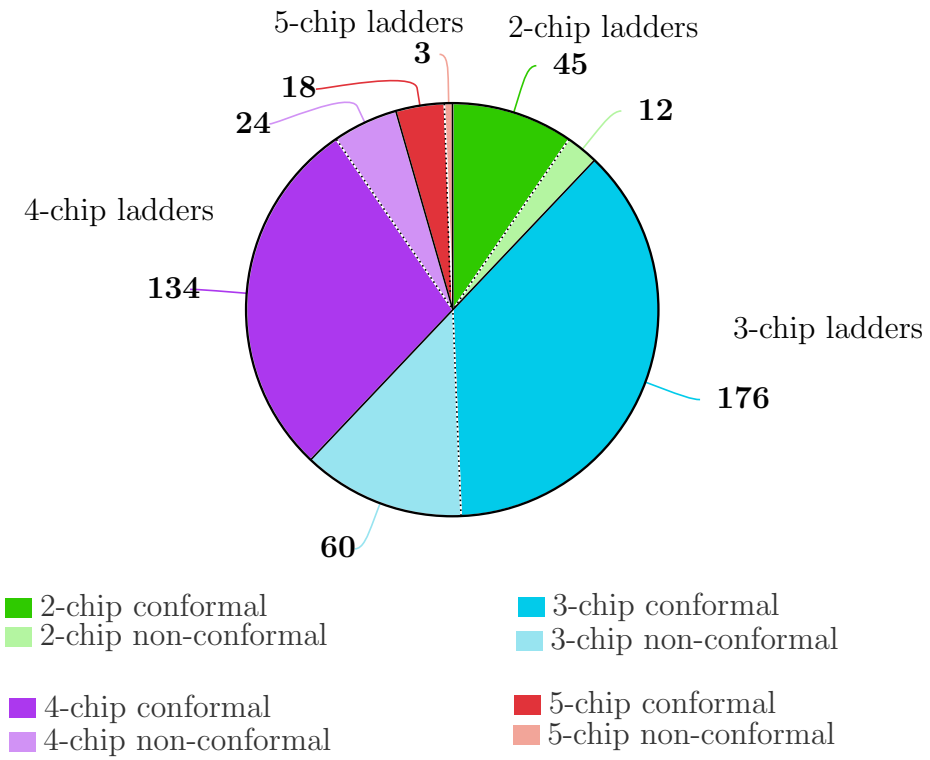


Fig. 6.1: A representation of the number of produced ladders with a different number of ALPIDE chips. The number of conformal and problematic ones is also shown.

6.1 Power consumption

This part of the analysis aims to explore the power consumption of the ladders. Electrical tests consisting of `test A, B` and `C` were further described in Chapter 5.

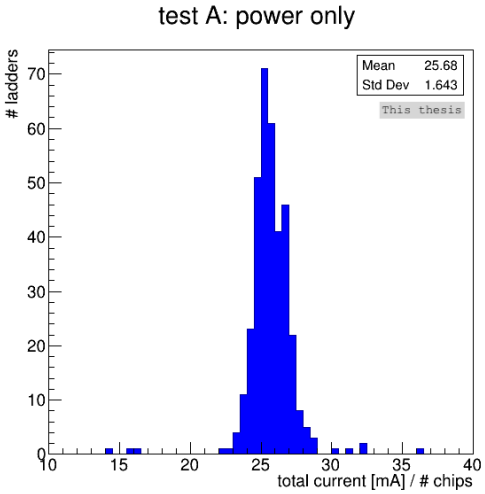
Starting with the data filled in the `LADDER_form`, the 30 mA had to be subtracted from all the results, as it represents the current consumption of the ICM card. To make plots clear and understandable, all the plots were normalised by the number of chips in the ladder.

In Fig. 6.2, we observe that applying the clock increases the average power consumption, which is expected since the clock activates the chip circuitry. However, there is a population of few ladders with a current of about 50-55 mA per chip, where we explored a hypothesis that the mentioned outliers could have been caused by the fact that two different MOSAIC boards were used. Although, after plotting just the data measured using only MOSAIC board `25:3d:75`, the shape of the distribution remained the same, including the presence of outliers. The power consumption should be therefore studied further.

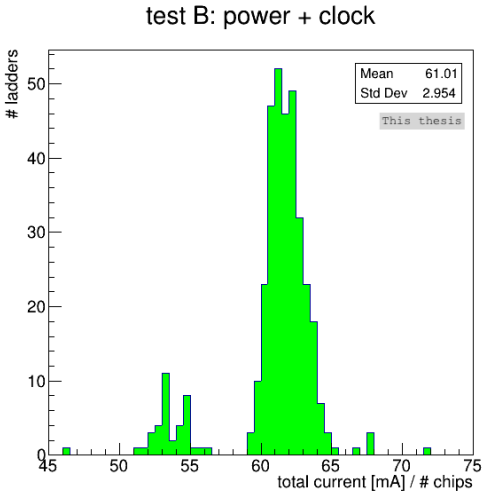
After applying the back-bias voltage $V_{\mathrm{BB}} = -3$ V, a current IBB of 7.7 mA was measured for the majority of ladders as shown in Fig. 6.3, with the acceptability criteria being IBB < 10 mA.

6.1.1 Power correlations

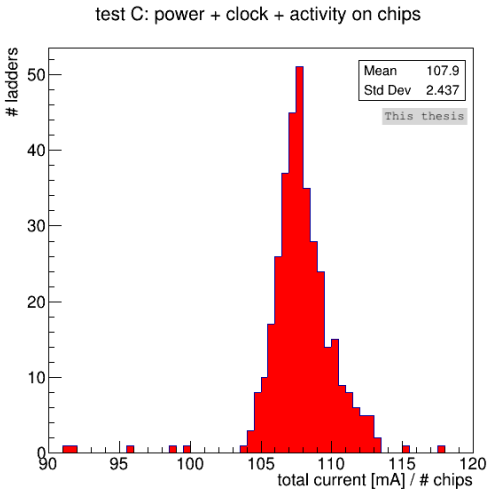
The problem with two separate populations can also be observed in the correlation plots, see Fig. 6.4. The cause of this behaviour is still under investigation.



(a)



(b)



(c)

Fig. 6.2: Results of electrical test: Power consumption of ladders is electrical tests A, B, and C.

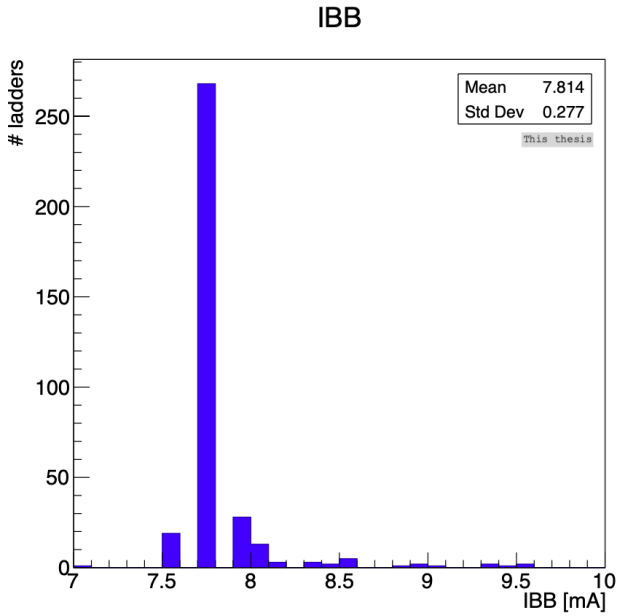
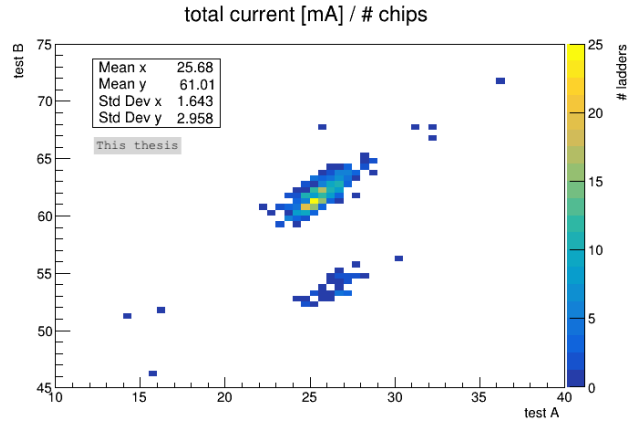
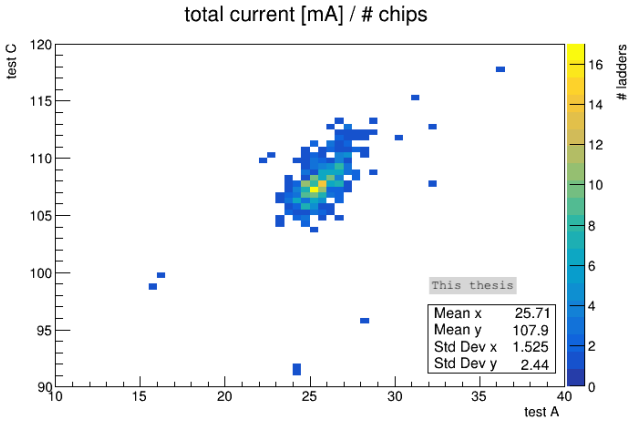


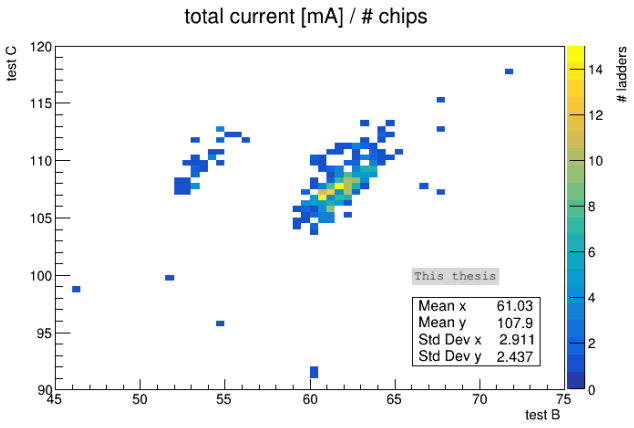
Fig. 6.3: Current consumption with back-bias voltage $V_{\mathrm{BB}} = -3$ V.



(a)



(b)



(c)

Fig. 6.4: Correlation plots of electrical tests: (a) Correlation between test A and B, (b) Correlation between test A and C, (c) Correlation between test B and C.

6.2 Threshold-noise characteristics

The threshold and noise distributions for ALPIDE chips in all types of ladders (2-, 3-, 4- and 5-chip ladders) were plotted. At first separately; after the same behaviour for all types was observed, the plots were merged and values for single chips were plotted. These include threshold mean, threshold deviation, noise mean, noise deviation, all with and without back-bias voltage $V_{\mathrm{bb}} = -3$ V.

6.2.1 Threshold characteristics

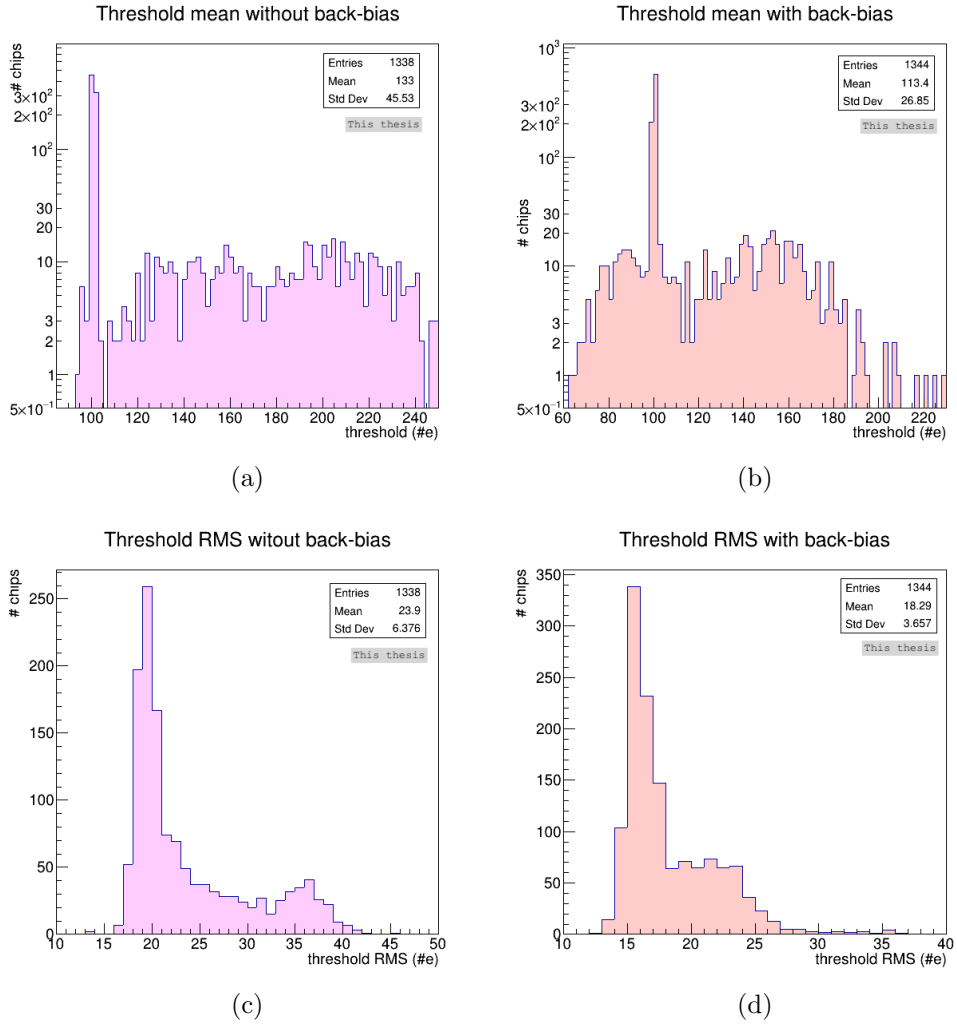


Fig. 6.5: Statistics on threshold values - threshold mean without back-bias (a), threshold mean with back-bias (b), threshold RMS without back-bias (c) and threshold RMS with back-bias (d).

The aim for the threshold is to be as uniform as possible. As we can see in plots in Fig. 6.5 (a) and (b), we observe peaks at 100 electrons both for $V_{\mathrm{BB}} = 0$ V and $V_{\mathrm{BB}} = -3$ V, which means the goal to achieve uniform threshold was achieved. In the distribution with back-bias voltage, some chips with a threshold below 100 electrons occurred.

For threshold RMS (in Fig. 6.5 (c) and (d)) without back-bias voltage, we observe a double-peak structure. The peak at $\sim$ 36 electrons could be explained by the presence of a lead solder blob on the kapton tape on the ladder—from lead decay chain, where electrons from lead decay (β^-) are entering the detector. Another explanation can be found in [49]: the threshold RMS can be larger than average pixel noise, i.e. the fixed-pattern noise (FPN) is larger than the temporal noise. The FPN originates from transistor mismatches in the in-pixel circuitry, thus causing pixel variations with a stable pattern.

Considering the most frequent value, we can see that the RMS mean is shifted to the left with adding V_{BB}.

6.2.2 Noise characteristics

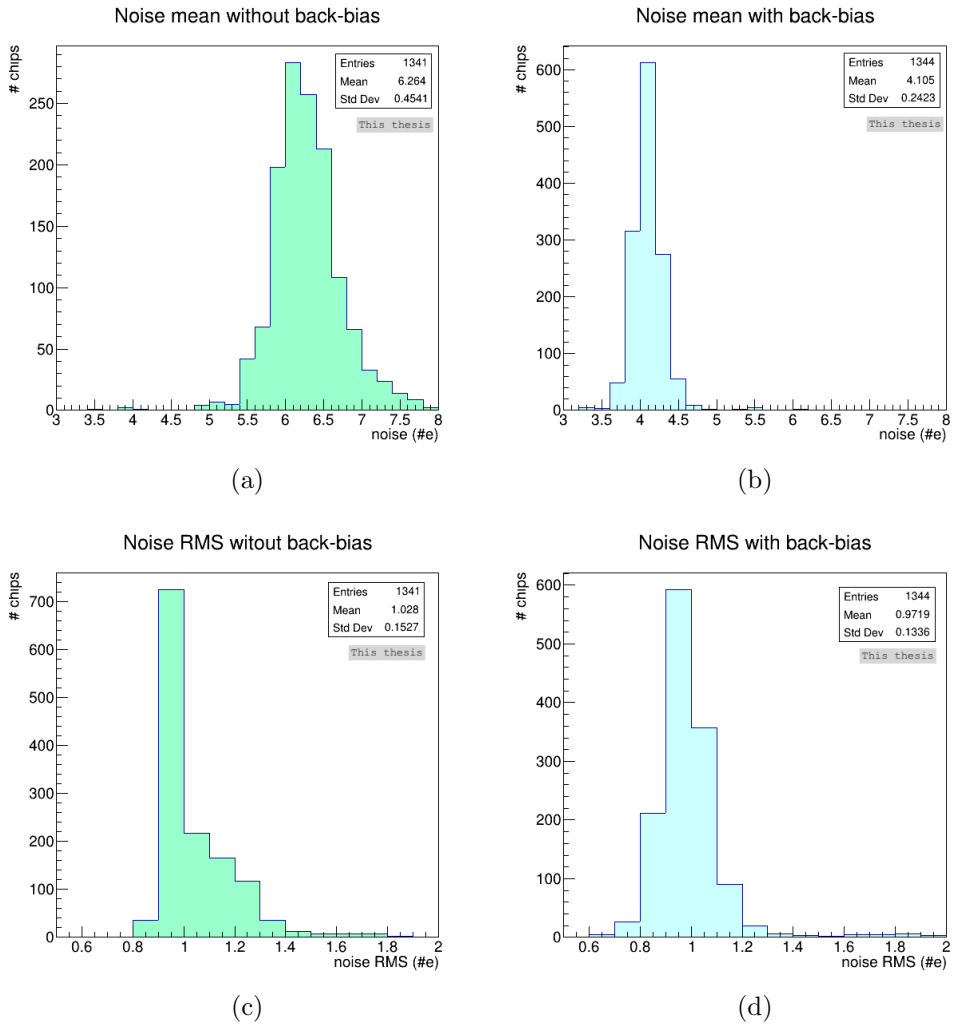


Fig. 6.6: Statistics on noise values - noise mean without back-bias (a), noise mean with back-bias (b), noise RMS without back-bias (c) and noise RMS with back-bias (d).

For average noise, as plotted in Fig. 6.6 (a), (b), the most frequent values are ~ 6 electrons, applying the back-bias voltage lowers the average noise to ~ 4 electrons.

To conclude, applying back-bias voltage reduces the noise and makes the threshold distribution more narrow, which is expected since the back-bias increases the depletion zone and therefore improves the S/B ratio of the charge collection diode.

6.3 Dead and noisy pixels

Analysis on the dead and noisy pixels has been done separately for the values obtained from the digital scan and the threshold scan. For inefficient pixels, the values are obtained only from the digital scan. In the digital scan, where the digital part of the circuit is qualified, each pixel is pulsed 50 times - a pixel is considered dead, if it does not respond at all, inefficient, if it responds between 1 and 49 times, and noisy, if more than 50 replies are received. In the threshold scan, the analog part of the chip is tested, exploring the value of injected charge at which the pixel starts to detect particles. Here, a dead pixel represents a pixel, where the threshold is unrealistically high and a noisy pixel has extremely low threshold.

6.3.1 Dead pixels

Data for dead pixels in a chip and as a sum of all chips in the ladder are plotted separately in Fig. 6.7 and 6.8. The highest peak is observed in the first bin, which is a satisfactory result. Another peaks can be seen at 500 (512) pixels, which corresponds to one full row, around 1000 (1024) and 2000 (2048) pixels, which could be explained be one full column or double-column of dead pixels respectively. There are no major differences between the number of dead pixels measured with $V_{\mathrm{BB}} = 0$ V or with $V_{\mathrm{BB}} = -3$ V.

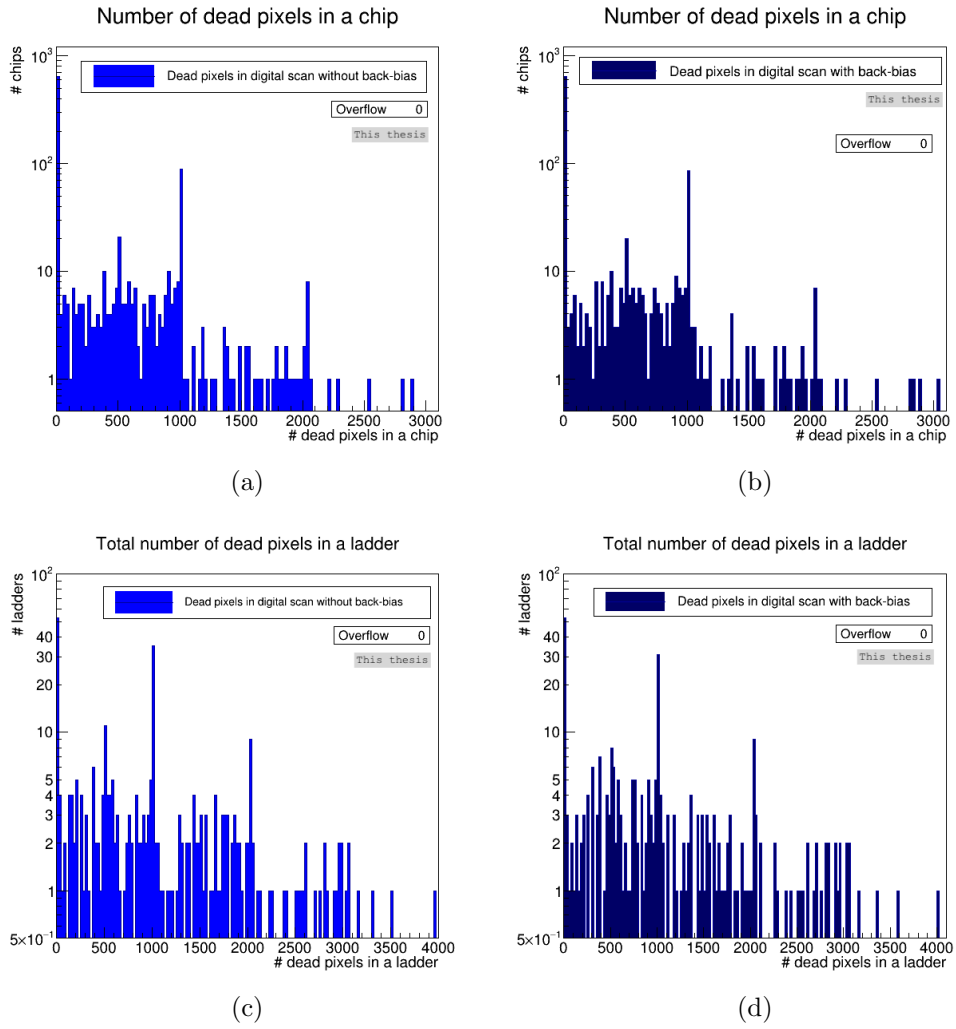


Fig. 6.7: Number of dead pixels per chip in digital scan with $V_{\mathrm{BB}} = 0$ V (a) and with $V_{\mathrm{BB}} = -3$ V (b). Number of dead pixels per ladder (sum of dead pixels in all the sensors) in digital scan with $V_{\mathrm{BB}} = 0$ V (c) and with $V_{\mathrm{BB}} = -3$ V (d).

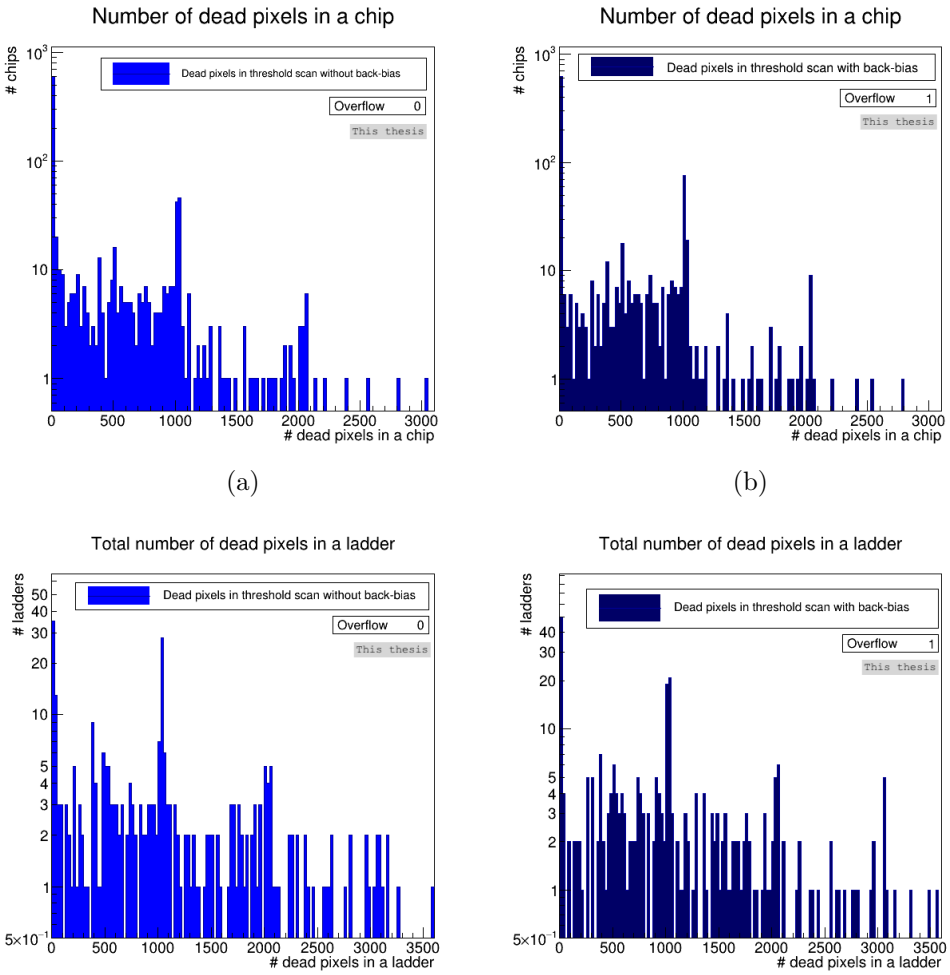


Fig. 6.8: Number of dead pixels per chip in threshold scan with $V_{\mathrm{BB}} = 0$ V (a) and with $V_{\mathrm{BB}} = -3$ V (b). Number of dead pixels per ladder (sum of dead pixels in all the sensors) in threshold scan with $V_{\mathrm{BB}} = 0$ V (c) and with $V_{\mathrm{BB}} = -3$ V (d).

6.3.2 Noisy pixels

For the number of noisy pixels, the result is satisfactory: a peak at zero is observed and there is a just a few ladders with more noisy pixels.

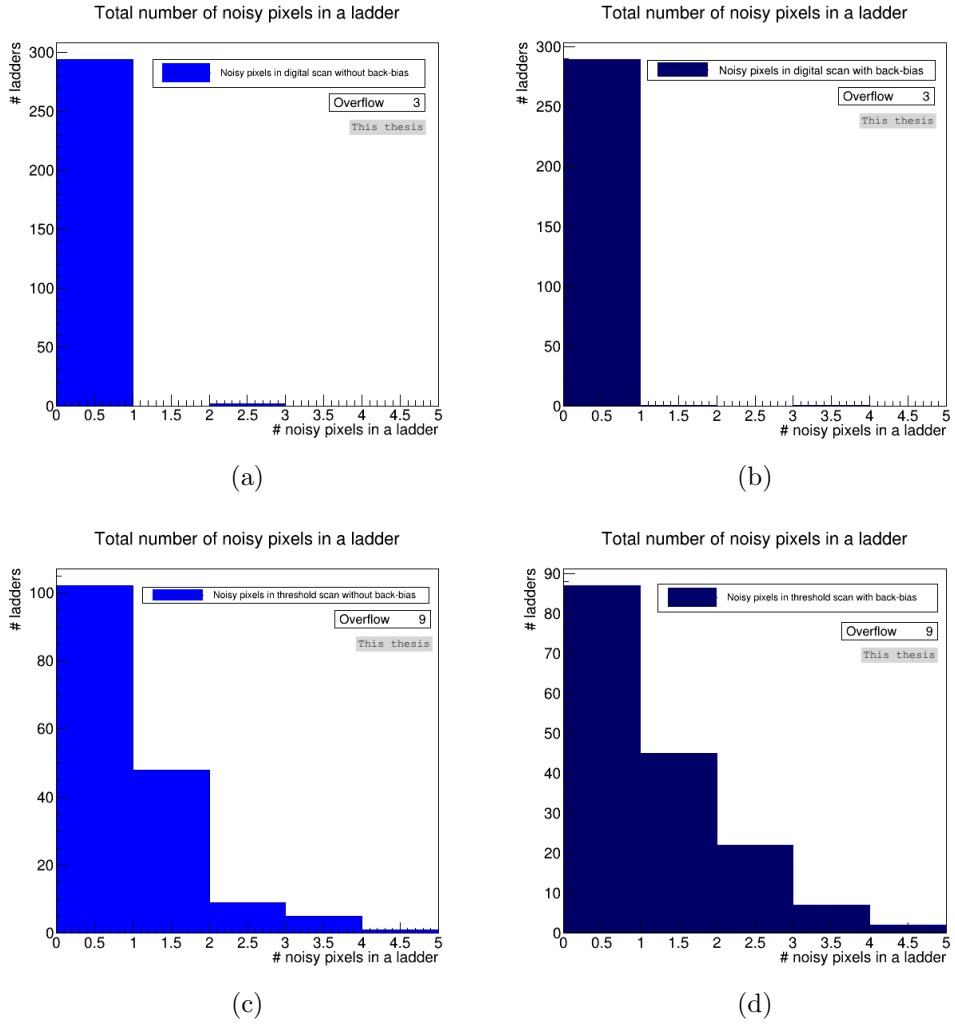
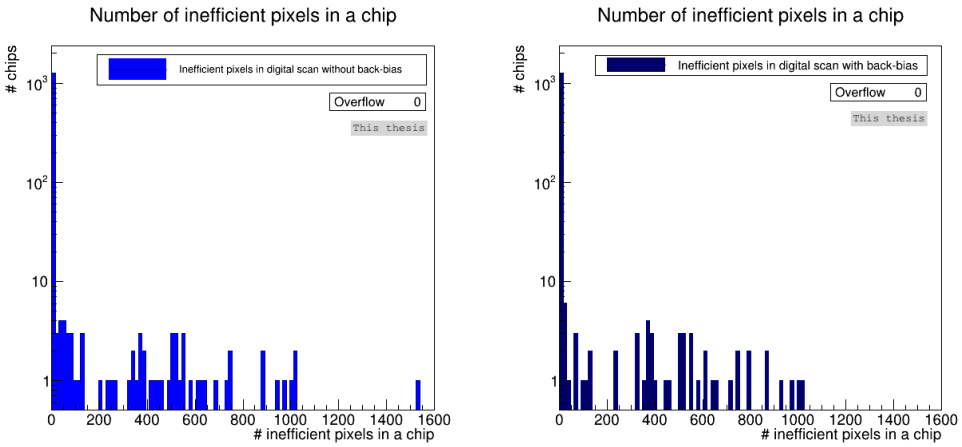


Fig. 6.9: Number of noisy pixels per ladder (sum of noisy pixels in all the sensors) in digital scan with $V_{\mathrm{BB}} = 0$ V (a) and with $V_{\mathrm{BB}} = -3$ V (b). Number of noisy pixels per ladder in threshold scan with $V_{\mathrm{BB}} = 0$ V (c) and with $V_{\mathrm{BB}} = -3$ V (d).

6.3.3 Inefficient pixels

The number of inefficient pixels is plotted in Fig. 6.10. A small number of chips contains more than zero inefficient pixels, although a few chips with about 512 and 1024 inefficient pixels occurred, corresponding to one full row or column respectively.



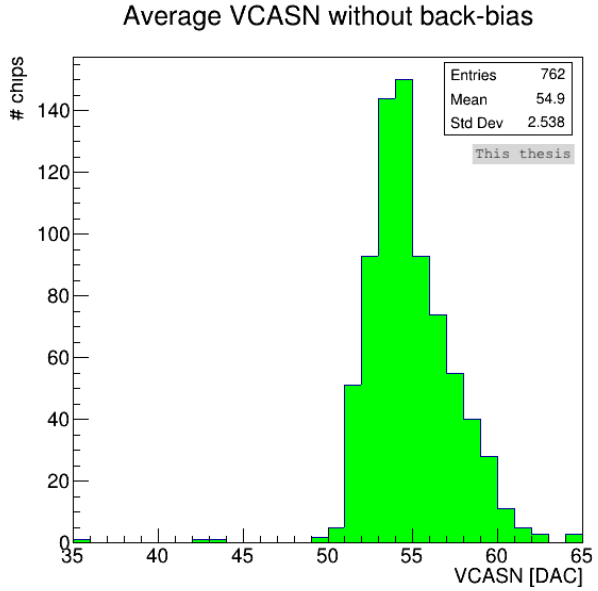
(a) (b)

Fig. 6.10: Number of inefficient pixels per chip in digital scan with $V_{\mathrm{BB}} = 0$ V (a) and with $V_{\mathrm{BB}} = -3$ V (b).

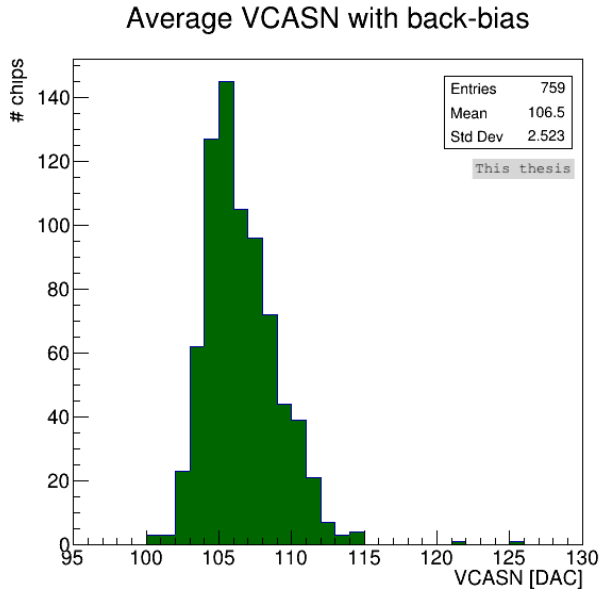
6.4 VCASN scan results

VCASN values were provided only for the part of ladders that have been tested.

In the VCASN distributions, a tail in the histogram is observed. This may be explained by the DAC calibration performed on the chip via the MAM probe card. For the VCASN distributions, we expect a symmetric Gaussian distribution. However, the obtained results provide a right-skewed distribution, which could be explained by the DAC coding of VCASN values. VCASN values are coded with 8-bit DAC. While performing the probe test in the MAM, DAC needs to stay linear, which is always true for small values. Although, at highest voltage values, the linearity was distorted for a few chips. The non-linear DAC calibration could therefore result in a tail seen in the histogram in Fig. 6.11, where the higher VCASN values were coded with a lower value.



(a)



(b)

Fig. 6.11: Measured values of the VCASN parameter in all the conformal ladders with $V_{\mathrm{BB}} = 0$ V and $V_{\mathrm{BB}} = -3$ V.

Chapter 7

Summary and outlook

The Run 3 at the LHC will be performed at a significantly higher luminosity, therefore the ALICE upgrade project consists of numerous improvements. Besides the upgraded hardware, including the new gas electron multipliers in the TPC, the silicon ALPIDE chips in both ITS and the MFT or the FIT detector, the data processing will also undergo a major change: from the trigger mode to continuous processing in a framework called O^2. This will allow us to perform new measurements with even higher accuracy.

This work was devoted to the commissioning of the MFT, a new detector which will allow precise vertexing capabilities to muon tracking at forward rapidity in ALICE. To clarify the basic motivation to add the forward tracking detector to the ALICE detector system, the current state of the experiment and the description of silicon detectors in general were presented in Chapters 1 and 2, respectively.

The MFT, consisting of 10 half-disks with 2 detection planes each, will use the ALPIDE silicon chips to detect high-energy particles. The ALPIDE sensors, used for both the ITS and the MFT after the upgrade, were presented in Chapter 3. The physics motivation for the MFT was described in the beginning of Chapter 4 and will be further elaborated in my diploma thesis, along with Monte Carlo simulations of particles produced in the forward direction.

The technical part of the work that I participated in CERN was presented in Chapter 5, where the specific procedures in the MFT commissioning were described. The statistical analysis of the qualification results was also performed to better understand the behaviour of the detector and can be found in Chapter 6.

Currently, the MFT is under tests on surface. The quality control development and calibration are ongoing. According to the current LHC schedule, the installation of the MFT is planned for December 2020 and January 2021. In May 2022, after the global commissioning and calibration will be done, the first LHC beams are expected to come to later bring exciting new physics discoveries.

Long-term outlook

After the next LHC shutdown in 2025, the ALICE detector system in the Run 4 will include FoCal, the system of forward electromagnetic and hadronic calorimeters and the ITS3 with the three innermost layers replaced. The interest to continue to improve the central silicon tracking detector in ALICE has been expressed in [50] and [51]. The ITS3 would be a novel vertex detector consisting of wafer-scale, ultra-thin MAPS in curved, perfectly cylindrical layers. The control logic, data buffers and links would be placed at the edge of the sensor.

According to ALICE upgrade simulations, the ITS3 will result in reduced combinatorial background from conversions, better charm rejection access to the most sensitive region for coalescence or better resolution on (anti-)deuteron impact parameter crucial to discriminate signal from background.

Concerning ALICE in the LHC Run 5 [52], as mentioned in the Update of the European strategy for particle physics, the ambition is to *design a new experiment to continue with a rich heavy-ion programme at the HL-LHC*. The goal for ALICE is to study pp, pA and AA collisions at luminosities 20-50$\times$ higher that in ALICE in Run 3-4. What was presented, would be a compact, all-silicon *nearly massless* detector with excellent low-p_T tracking capabilities. The innermost layers would be placed possibly inside the beam pipe.

The silicon detectors in general will obviously play an important role in the future of HEP. The work at the MFT, which is a prominent example of where the current silicon technology stands, is a great experience for me as a particle physicist to use the acquired knowledge and, by learning how to detect the elementary particles, allows me to acquire deeper understanding of what the particles actually represent.

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